CS/ECE 755: VLSI Design
Department of Computer Sciences
University of Wisconsin-Madison

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Examination I
In-Class
Tuesday, October 14, 2008
Weight: approximately 17.5%

1 hour 15 minutes
Open book, open notes.
Exam is one-sided, total of 11 numbered pages. Plan your time carefully.
One blank page included in the end for rough work. Also use left-side blank pages for rough work.
NAME: _______________________
Email: _______________________

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Part 1: Multiple choice (3x4 = 12 points)

The following problems have one or more correct responses. Circle ALL correct answers.

1) Interconnect noise can be reduced with
   a) Wider wires
   b) Wider spacing
   c) Shielding
   d) Repeaters

2) P/N ratio for transistors in the combinational gates depend on
   a) Input arrival times
   b) Mobility (μ)
   c) Whether gate is high-skew or low-skew
   d) Whether gate is used in a pulse-based, latch-based, or flip-flop based design

3) Funnel shifter using pass nMOS pass transistors:
   a) Have delay linearly proportional to N
   b) Suffer threshold drop problems
   c) Have high parasitic capacitance
   d) Scale to large N because of regular layout

4) Which of the following statements is true about noise margins
   a) Noise margin are defined at the unity-gain slope points
   b) Reducing noise margins increase gate delay
   c) Noise margin is independent of Vdd
   d) Increasing the beta ratio increases the LOW noise margin
Part 2: Transistor sizing (20 points)
Size the transistors in the circuit below so that it has the same drive strength in the worst case, an inverter that has PW=3 and NW=2. Use smallest possible widths to achieve this ratio. Write the sizes next to the transistors. For partial credit, show your work.
Part 3: Elmore delays (20 points)

Use the Elmore delay approximation to find the worst case fall delay at the output for the circuit below. Under what scenario does best case delay occur? Assume the following:

a) Diffusion capacitance is equal to the gate capacitance
b) Minimum sized transistor has gate capacitance = C, and diffusion capacitance = C

c) Resistance of NMOS transistor is R
d) No sharing in diffusion regions

Show your RC circuit first and your work for partial credit.

Final Answer:
Provided with HWS Solution Set.
Part 4: Logical effort (20 points)

Find the size of the transistors for the circuit below for minimum delay from input to output using logical effort. Annotate the individual sizes for the AOI21 gate.

Assume G1 is given

\[ G = 1 \times \frac{2}{3} \times \frac{2}{3} \times 4 = 144/27 \]

\[ B = 1 \times 4 \times 1 \times 1 = 4 \]

\[ H = 45/3 \]

\[ P = 1 + 3/3 + 4 + 2 = 9.3 \]

\[ F = G + B \cdot H = 319.8 \]

\[ I = \sqrt{F} = 4.22 \]

\[ G_{AI} = (45) \cdot (4/3) = 14.2 \]

\[ G_{AI} \text{ is a NAND} \]

\[ P + N = 14.2 \Rightarrow P = N = 7 \]

\[ G_{A} = (14) \cdot (6/3) = 6.63 \]

\[ \frac{6.63}{4.22} \]
G_3 is a 4 input NAND gate. 

Now, consider sizing G_3 one input:

\[ P + N = 14 \]
\[ P_W = \frac{1}{2} N_W. \quad \text{because} \quad P_{\text{MOS}} = 2, \quad N_{\text{MOS}} = 4 \]

\[ \frac{1}{2} N_W + N_W = 6.63 \]
\[ \Rightarrow N_W = 4.22, \quad P_W = 2 \]

\[ \text{cin}_{G_{12}} = (6 \times 4) \cdot \frac{6}{3} = 11.37 \]
\[ \frac{4.22}{4.22} \]

Consider input \( q_1 \), \( N_W = 2, \quad P_W = 4 \)

To size its transistors:

\[ 2N_W + N_W = 11.37 \]
\[ N_W = 3.79 \approx 4 \]
\[ P_W = 8 \]

Consider inverter:

\[ \text{cin}_{G_{1}} = \frac{12.1}{4.22} = 2.843 \approx 3 \]
\[ P + N = 3. \quad \text{Matches our assumption.} \]
Part 5: Standard cells (20 points)

Using logical effort or with detailed simulation we can size individual transistor sizes and decide the number of stages for any logic path. Thus, for a given circuit there is a large design space to explore to determine the best solution. However standard cell based designs provide just one or two sizes for each gate and synthesis tools map the design to these gates. I am going to argue that standard cell based design does NOT deviate significantly from a full-custom detailed transistor sizing approach. Justify or discredit my claim ☹️

The optimal number of stages to minimize delay falls in a shallow curve

Thus deviating from number of stages by using a std. cell approach will not result in that much loss.
Part 6: Stick diagrams (20 points)

Shown below is the schematic and the stick diagram of a 6-transistor SRAM cell. Estimate the height of the cell. Assume standard design rules adopted for the course. Show all of your work!

Simple solution: $6\lambda$ and $7$ tracks $\Rightarrow 42\lambda$

(considering all rules; see annotated diagram)
Part 7: Qualitative analysis (2x10 = 20 points)

On the left are 10 descriptions of graphs describing different trends labeled a-j. On the right are 10 graphs. Match each description with a graph that shows the trend and fill in the table below. You can reuse graphs and not all graphs are used at least once.

a. Delay of inverter vs. output load
b. Delay of inverter vs. transistor width (fixed output load)
c. Wire capacitance per unit-length vs wire width
d. Wire delay vs. Length (unbuffered wire)
e. Wire delay vs. Length (buffered wire)
f. Saturation current vs. Transistor width
g. Max current vs. supply voltage for nMOS transistor
h. Voltage vs. gate capacitance
i. Optimal sizing (P/N ratio) for unskewed gate vs mobility

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