1) (a) \[ ac + bdc + c\bar{a} = (a + \bar{a})c + bdc = c(1 + bd) = c \]
   (b) \[ (x + y)(x + z) = x + xz + xy + yz = x(1 + yz) + yz = x + yz \]
   (c) \[ a(b + c + d) + b(c + d + a) + c(d + a + b) + d(a + b + c) \]
   \[ = ab + ac + ad + bc + bd + ab + cd + ac + bc + ad + bd + cd \]
   \[ = ab + ac + bc + ad + bd + cd \]

2) 

3) The answer for this problem can be different.
   (a) Implementation using 4-to-1 mux:
Implementation using 2-to-1 mux:

Implementation of gate-level 2-to-1 mux:

Full gate-level implementation of the logic:
(b) The # of transistors for a 2-to-1 mux: $3 \times 4 + 1 \times 2 = 14$
   
   The # of transistors for a 4-to-1 mux (three 2-to-1 muxes): $14 \times 3 = 42$
   
   another possible answer can be 60, if you didn’t optimize 2-to-1 mux.

(c) A 2-to-1 mux can be implanted with 2 transmission gates and 1 inverter. Thus the # of transistors needed is $(2 + 2 + 2) \times 3 = 18$

This layout is a 2-to-1 mux implemented by 2 transmission gates.

The cell is easy to tile in the **VERTICAL** direction for 2 reasons:

(1) Easy to route select signals $c$ and $c'$, if multi-bit wide 2-to-1 muxes are implemented by using this layout.

(2) Easy to connect I/O signals from one stage to another (a stage consists of a group of vertical tiled muxes and place stages horizontally).