1. Problem 4.3 from the Exercises for Chapter 4 (This solution is using AOI21)

The worst case rising delay happens when one of A and B turn on and C turn on.
The resistance of width-4 PMOS is R/2 if we assume the resistance of width-2 PMOS is R. Also, the resistance of width-1 NMOS is R.
Using Elmore delay model, the rising delay is \((R/2)*(4C+4C) + (R/2+R/2)*(4C+2C) = 10RC\)
The worst case falling delay is happened when B turn on before A turn on.
The falling delay is \((R/2)*C+(R/2+R/2)*(2C+4C) = 6.5RC\).
(The answer is based on the transistor schematic and the stick diagram you draw. The capacitance values depend on your layout design.)

2. Problem 4.4 from the Exercises for Chapter 4
The output node has capacitance of $3\text{nC}$ ($2\text{nC}$ from pull-up network and $1\text{nC}$ from pull-down network), and each internal node has $2\text{nC}$. The resistance through each pMOS is $R/n$. The propagation delay is:

$$t_{pd} = R(3\text{nC}) + \sum_{i=1}^{n} \left( \frac{iR}{n} \right) (2\text{nC}) = \left( n^2 + 2n \right) RC$$

3. Problem 4.10 from the Exercises for Chapter 4
(a) should be faster than (b) because the NAND has the same parasitic delay but lower logical effort than the NOR.

In each design, $H = 6$, $B = 1$, $P = 1 + 2 = 3$.

For (a), $G = (4/3) \times 1 = 4/3$. $F = GBH = 8$. $f = 8^{1/2} = 2.8$.

$$D = 2f + P = 8.6\tau.$$  
So, $x = 6C \times 1/f = 2.14C$.

For (b), $G = 1 \times (5/3)$. $F = GBH = 10$. $f = 10^{1/2} = 3.2$.

$$D = 2f + P = 9.3\tau.$$  
So, $y = 6C \times (5/3)/f = 3.16C$.

4. Problem 4.11 from the Exercises for Chapter 4
\[ D = N(GH)^{1/N} + P, \quad B=1 \]

<table>
<thead>
<tr>
<th>Design</th>
<th>( G )</th>
<th>( P )</th>
<th>( N )</th>
<th>( D(H=1) )</th>
<th>( D(H=5) )</th>
<th>( D(H=20) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>( \frac{8}{3} \times 1 )</td>
<td>6 + 1</td>
<td>2</td>
<td>10.3</td>
<td>14.3</td>
<td>21.6</td>
</tr>
<tr>
<td>(b)</td>
<td>( \frac{5}{3} \times \frac{5}{3} )</td>
<td>3 + 2</td>
<td>2</td>
<td>8.3</td>
<td>12.5</td>
<td>19.9</td>
</tr>
<tr>
<td>(c)</td>
<td>( \frac{4}{3} \times \frac{7}{3} )</td>
<td>2 + 3</td>
<td>2</td>
<td>8.5</td>
<td>12.9</td>
<td>20.8</td>
</tr>
<tr>
<td>(d)</td>
<td>( \frac{5}{3} \times \frac{1}{3} \times \frac{4}{3} \times 1 )</td>
<td>3 + 1 + 1 + 1</td>
<td>4</td>
<td>11.8</td>
<td>14.3</td>
<td>17.3</td>
</tr>
</tbody>
</table>

The more stages you have, the more electrical effort can be distributed over the stages.

So, when \( H \) is large, the design which has more stages is faster.

5. Problem 4.13 from the Exercises for Chapter 4
Assumptions: XOR gate has \( g=p=4 \), and neglecting the branch on A which could be buffered.

\[ G = 4 \times \left( \frac{9}{3} \right) \times \left( \frac{6}{3} \right) \times \left( \frac{5}{3} \right) = 40 \]
\[ B=16 \text{ driving the final ANDs.} \]
\[ H=\frac{10}{10}=1 \]
\[ \text{Path Effort } F=GBH=640. \]
\[ N=4, \text{ Best stage effort } f=(640)^{1/4} = 5.03. \]
\[ P=4+4+4+2=14 \]
\[ D=Nf+P = 34.12\tau = 6.8 \text{ FO4 delays.} \]

Input capacitances,
\[ z = 10 \times \left( \frac{5}{3} \right) / 5.03 = 3.18; \quad y = 16 \times z \times \left( \frac{6}{3} \right) / 5.03 = 20.27; \quad x = y \times \left( \frac{9}{3} \right) / 5.03 = 12.09. \]
6. (1)

The PMOS width of given inverter is 3 and the NMOS width of given inverter is 2. So, the PMOS resistance is $1/3$ and the NMOS resistance is $1/2$.

In order to make same pull-up and pull-down network of inverter, we can size the PMOS and NMOS as above figure.

- Pull-up network resistance: $(1/9 + 1/9) + 1/9 = 3/9 = 1/3$. (Only consider A, B, and (D or E)), $1/5 + 1/9 = 14/45 \approx 1/3$ (Only consider C and (D or E))
- Pull-down network resistance: $1/4 + 1/4 = 1/2$. (Only consider ((A or B) and C) or (D and E))

(2) Another possible PMOS sizing is: $A = B = 12$; $C = D = E = 6$
(a) Assume that all load and internal capacitances have been charged to $V_{DD}$. Which input vector will result in the longest $t_{pdf}$?

Sol) Diffusion capacitance of each transistor is shown in the above figure. There are two routes to discharge load and other capacitance. One route is through C.D, and E. The other one is through A and B.

If $A=B=1$, load capacitance will be discharged through the A and B, and the discharge will be faster than the other route because there are only 2 transistors. Turning on A will increase delay because diffusion capacitance of A(source) and B(drain) should be discharged through C,D, and E.

So, maximum delay would be happened when $ABCDE=10111$. This presents the maximum capacitance to the output node.

(b) Assuming all the capacitors are initially charged to $V_{DD}$, use the Elmore delay approximation to find the value of $t_{pdf}$ for the input vector $ABCDE = 10111$. 
\[ t_{\text{pHL}} = (20f \times 5k) + (15f \times 10k) + (20f \times 20k) + (50f \times 15k) = 1.4nS \]