CS755 VLSI Design

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Homework #3

Assigned: September 29th, 2009         Due: October 13th, 2009

1. Find the rising and falling propagation delays of an AND-OR-INVERT gate using the Elmore delay model. Estimate the diffusion capacitance based on a stick diagram of the layout.
   (Problem 4.3 from the Exercises for Chapter 4)

2. Find the worst-case Elmore parasitic delay of an $n$-input NOR gate.
   (Problem 4.4 from the Exercises for Chapter 4)

3. Consider the two designs of a 2-input AND gate shown in the following figure. Give an intuitive argument about which will be faster. Back up your argument with a calculation of the path effort, delay, and input capacitances $x$ and $y$ to achieve the delay.
   (Problem 4.10 from the Exercises for Chapter 4)

4. Consider the four designs of a 6-input AND gate shown in the following figure. Develop an expression for the delay of each path if the path electrical effort is $H$. What design is fastest for $H = 1$? For $H = 5$? For $H = 20$? Explain your conclusions intuitively.
   (Problem 4.11 from the Exercises for Chapter 4)
5. Design a circuit at the gate level to compute the following function:
   if (a == b)  y = a;
   else y = 0;
   Let $a$, $b$, and $y$ be 16-bit buses. Assume the input and output capacitances are each 10 units. Your goal is to make the circuit as fast as possible. Estimate the delay in FO4 inverter delays using Logical Effort if the best gate sizes were sized. What sizes do you need to use to achieve this delay?
   (Problem 4.13 from the Exercises for Chapter 4)
   (Hint: Try a design with 4 stages; 2-bit XNOR gates to check for bitwise equality, a 16-input AND function to check equality of the input words (using 4-input gates, for example), and an AND gate to choose between Y and 0).

6. Size the following gate so that it has the same drive strength as an inverter that has a pMOS transistor of width 3 and an nMOS transistor of width 2.
7. The n-channel transistors in the following portion of a CMOS circuit have an on-resistance of 5 kΩs. The total source and drain (diffusion) capacitances of an n-channel transistor are 5 fF each. The parasitic (wiring, etc.) capacitances are shown lumped at the internal nodes. The output load capacitance shown (50 fF) includes the diffusion capacitance of the P-Network, wiring capacitances, and the driven gate capacitances.

(a) Assume that all load and internal capacitances have been charged to $V_{DD}$. Which input vector will result in the longest $\tau_{pdf}$? Explain your answer.

(b) Assuming all the capacitors are initially charged to $V_{DD}$, use the Elmore delay approximation to find the value of $\tau_{pdf}$ for the input vector ABCDE = 10111.