1. Problem 4.20 from the Exercises for Chapter 4

(1) k-input NAND

Sol) Logical effort of k-input NAND: \( g = \frac{\mu+k}{\mu+1} \);

Logical effort of k-input NOR: \( g = \frac{\mu k+1}{\mu+1} \).

As \( \mu \) increases, NOR gates get worse compared to NAND gates because the series pMOS devices become more expensive.

2. Problem 4.25 from the Exercises for Chapter 4

Sol) If the first upper inverter has size \( x \) and the lower \( 100-x \) and the second upper inverter has the same stage effort as the first (to achieve least delay), the least delays are

\[ D = 2\left(\frac{300}{x}\right)^{1/2} + 2 = \frac{300}{100-x} + 1. \]

Hence \( x = 49.4 \), \( D = 6.92 \tau \)

If we assume the size of the second upper inverter is \( y \), \( 300/y = y/x \). \( y^2 = 300*49.4 \). \( y = 121.7 \)

In sum, the sizes are 49.4 and 121.7 for the upper inverters and 50.6 for the lower inverter.

Such circuits are called forks and are discussed in depth in [Sutherland99].
3. Problem 6.12 from the Exercises for Chapter 6

\[ n_{crit} = 1. \] For \( g_{crit} = 1.5 \), \( C_{in} = 4.5 \), so \( \rho_{crit} = 4.5-1 = 3.5 \) on the critical input. For unit resistance, \( R = 2/\rho_{crit} + 2/(2/\rho_{noncrit}) = 1 \rightarrow \rho_{noncrit} = 4/(1-2/\rho_{crit}) = 28/3 \). If \( n_{noncrit} = 1/2 \), \( g_{noncrit} = (\rho_{noncrit} + n_{noncrit}) / 3 = 3.28 \).

4. Problem 6.14 from the Exercises for Chapter 6

\( \rho(1, \rho/g) \) is the value of \( \rho \) satisfying \( \rho/g + \rho(1 - \ln \rho) = 0 \). Suppose we have a path with \( n_1 \) stages, a path effort \( F \), and a path parasitic delay \( P \). If we add \( N-n_1 \) buffers of parasitic delay \( \rho \) and logical effort \( g \), the best path delay is

\[ D = N \left( Fg^{N-n_1} \right)^{1/N} + P + (N-n_1)\rho \]

Differentiate this path delay with respect to \( N \) to find the number of stages that minimizes delay. The best stage effort at this number of stages is \( \rho(g, \rho) = (Fg^{N-n_1})^{1/N} \). Substituting this into the derivative and simplify to find

\[ \frac{\partial D}{\partial N} = \left( Fg^{N-n_1} \right)^{1/N} \left( 1 + \frac{n_1 \ln g}{N} - \frac{\ln F}{N} \right) + \rho = 0 \]

\[ \rho(g, \rho) \left[ 1 - \ln \frac{\rho(g, \rho)}{g} \right] + \rho = 0 \]

Assume the equality we are trying to prove is true and substitute it into the equation above to obtain

\[ \rho(1, \rho) \left[ 1 - \ln \rho(1, \rho) \right] + \frac{\rho}{g} = 0 \]

This is just the definition of \( \rho \) that we began with, so the substitution must have been valid and the equality is proven.
5. This problem is to design a fast **addition circuit (+)** to add a 32-bit number with a 4-bit number (to produce a 33-bit number). The circuit should be designed with two macros (shown below): an adder macro (adds numbers of a specified bit-width) which produces an adder with a delay of 100 pS/bit, and a multiplexer (which selects from inputs of specified bit width) which has a delay of 100 pS (independent of the size). The arrival times of the input signals to the circuit are also shown below.

![Adder and MUX Diagram]

Design the circuits for the following specifications, and show the interconnection of the modules below to meet the specs. Make sure that the you show the appropriate bits for the inputs to the modules. (You may not need to use all the modules for a solution, or you may need to add additional modules. Do NOT add any other logic other than the two modules.)

(a) Design a circuit to complete the addition in \(\leq 3\) nS.

![Circuit Diagram for <= 3 nS]

(b) Design a circuit to complete the addition in \(\leq 2\) nS.

The solution follows the same approach as above. The adder is split into three blocks (31:18, 17:4, 3:0). The carry out from the 17:4 block controls a mux which selects the appropriate
result from the 31:18 block. The carry out from the 3:0 block controls this mux as well as one which selects the appropriate result from the 17:4 block. This addition can be done in 1.6 nS.

6. Problem 4.19 from text
NAND2: \( g = 5/4 \); NOR2: \( g = 7/4 \). The inverter has a 3:1 P/N ratio and 4 units of capacitance. The NAND has a 3:2 ratio and 5 units of capacitance, while the NOR has a 6:1 ratio and 7 units of capacitance.