1. Problem 6.28 from the Exercises for Chapter 6.

The worst case is when A is low on one cycle, B, C, and D are high, and all the internal nodes become predischarged to 0. Then D falls low during precharge. Then A goes high during evaluation. The NAND has 11 units of capacitance on Cout precharged to VDD and 7.5 units of internal capacitance (C1, C2, C3) that will be initially low. The output will thus droop to $11/(11+7.5) VDD = 0.59 VDD$.


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The droop is \( \frac{6+5h}{6+5h+7.5} \). Charge sharing is less serious at high fanout.

With a secondary precharge transistor, one of the internal nodes is guaranteed to be high rather than low. Thus \( 11 + 2.5 = 13.5 \) units of capacitance are high and 5 units are low, reducing the charge sharing noise to \( \frac{13.5}{13.5 + 5} \) VDD = 0.73 VDD.