Standard Cell Layout Specification

CS755 VLSI Design

This document defines the layout fashion of the standard cell you are designing in the mini-project 1. All the layout designs have to follow this specification to create a unified standard cell library.

All the cells’ layouts in the library must have the height of 11.52 um as shown in the Fig. 1. A M1- POLY contact must be created for each pin and use metal 1 to wire the inputs to the cell input positions as illustrated in Fig. 2a. The first input (ip1) must be positioned at 5.4 um vertically from the bottom of the cell as illustrated in Fig. 2. Then the rest of the inputs, if have, must be positioned right below the ip1 with a spacing of 3.6 um and width of 3.6 um following the numerical sequence (ip1, ip2, ip3 ...) as shown in Fig. 2a. Fig. 2b shows how to place inputs in an extreme case.

Two power rails, vdd & gnd, must be drawn according to Fig. 3 and Fig. 4 respectively. All the taps have to be located within the rails (Metal 1). The height of both rails (Metal 1) is fixed at 0.99 um. The horizontal lengths of both rails must be the same for one cell. The vertical edges of two active regions of two taps must overlap with their corresponding rails’ edges, and the heights of both active regions are 0.36 um as illustrated in two figures. Also, the spacing between the top edge of n active region and the top edge of vdd rail is fixed at 0.36 um, and the spacing of the top edge of p active region and gnd rail is fixed at 0.315 um. The p/n select have to perturb the rails horizontally by 0.18 um. The dimension of both tap contacts (black square) are 0.18 um by 0.18 um, and the spacing between two contacts are fixed at 0.36 um. The spacing between vertical rail edge and the nearest tap contact is fixed at 0.18 um, and a cell may have to be widened or narrowed to meet this requirement. There has to be at least 0.36 um spacing for n-well all around the active regions within the well. For detailed spacing, refer to Fig. 3 and Fig. 4.

It may be better to draw all taps manually for this project. It is easy to adjust and gives cleaner layouts. A ntap has 5 layers – cc(contact), metal 1, nactive, nselect, and nwell. A ptap has 4 layers – cc, metal 1, pactive and pselect. Layer of metal 1 can be ignored here, since all the taps are under metal 1 power rail. Please refer to Fig. 3 and Fig. 4 for the spacing rules.
Fig. 2 Positions of Cell Inputs. (a) general case; (b) extreme case.
Fig. 3 Vdd Rail & Ntap
Fig. 4 GND Rail & Ptap