18. Circuit Design Pitfalls

- This module
  - Circuit pitfalls
  - Noise budgets
  - Reliability
Bad Circuit 1

- **Circuit**
  - 2:1 multiplexer

- **Symptom**
  - Mux works when selected D is 0 but not 1
  - Or fails at low $V_{DD}$
  - Or fails in SFSF corner

- **Principle: Threshold drop**
  - X never rises above $V_{DD} - V_t$
  - $V_t$ is raised by the body effect
  - The threshold drop is most serious as $V_t$ becomes a greater fraction of $V_{DD}$

- **Solution: Use transmission gates, not pass transistors**
**Bad Circuit 2**

- **Circuit**
  - Latch

- **Symptom**
  - Load a 0 into Q
  - Set $\phi = 0$
  - Eventually Q spontaneously flips to 1

- **Principle: Leakage**
  - X is a dynamic node holding value as charge on the node
  - Eventually subthreshold leakage may disturb charge

- **Solution: Staticize node with feedback**
  - Or periodically refresh node (requires fast clock, not practical processes with big leakage)
Bad Circuit 3

- **Circuit**
  - Domino AND gate

  ![Circuit Diagram]

- **Symptom**
  - Precharge gate \((Y=0)\)
  - Then evaluate
  - Eventually \(Y\) spontaneously flips to 1

- **Principle: Leakage**
  - \(X\) is a dynamic node holding value as charge on the node
  - Eventually subthreshold leakage may disturb charge

- **Solution: Keeper**
Bad Circuit 4

• Circuit
  – Pseudo-nMOS OR

  A  B  X  Y

• Symptom
  – When only one input is true, Y = 0
  – Perhaps only happens in SF corner

• Principle: Ratio Failure
  – nMOS and pMOS fight each other.
  – If the pMOS is too strong, nMOS cannot pull X low enough.

• Solution: Check that ratio is satisfied in all corners
Bad Circuit 5

- **Circuit**
  - Latch

- **Symptom**
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.

- **Principle: Ratio Failure (again)**
  - Series resistance of D driver, wire resistance, and tgate must be much less than weak feedback inverter.

- **Solutions: Check relative strengths**
  - Avoid unbuffered diffusion inputs where driver is unknown
Bad Circuit 6

- Circuit
  - Domino AND gate

  ![Domino AND gate diagram]

- Symptom
  - Precharge gate while
    - $A = B = 0$, so $Z = 0$
  - Set $\phi = 1$
  - $A$ rises
  - $Z$ is observed to sometimes rise

- Principle: Charge Sharing
  - If $X$ was low, it shares charge with $Y$

- Solutions: Limit charge sharing
  \[ V_x = \frac{C}{C_x + C_Y} V \]
  - Safe if $C_Y \gg C_X$
  - Or precharge node $X$ too
Bad Circuit 7

• Circuit
  – Dynamic gate + latch

• Symptom
  – Precharge gate while transmission gate latch is opaque
  – Evaluate
  – When latch becomes transparent, X falls

• Principle: Charge Sharing
  – If Y was low, it shares charge with X

• Solution: Buffer dynamic nodes before driving transmission gate
Bad Circuit 8

- **Circuit**
  - Latch

- **Symptom**
  - Q changes while latch is opaque
  - Especially if D comes from a far-away driver

- **Principle: Diffusion Input Noise Sensitivity**
  - If \( D < -V_t \), transmission gate turns on
  - Most likely because of power supply noise or coupling on D

- **Solution: Buffer D locally**
Bad Circuit 9

- **Circuit**
  - Anything

- **Symptom**
  - Some gates are slower than expected

- **Principle: Hot Spots and Power Supply Noise**
Noise

• Sources
  – Power supply noise / ground bounce
  – Capacitive coupling
  – Charge sharing
  – Leakage
  – Noise feedthrough

• Consequences
  – Increased delay (for noise to settle out)
  – Or incorrect computations
Reliability

- Hard Errors
- Soft Errors

<table>
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<th>Infant Mortality</th>
<th>Useful Operating Life</th>
<th>Wear Out</th>
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Electromigration

• “Electron wind” causes movement of metal atoms along wires

• Excessive electromigration leads to open circuits

• Most significant for unidirectional (DC) current
  – Depends on current density $J_{dc}$ (current / area)
  – Exponential dependence on temperature

  – Black’s Equation:
    $$ MTTF \propto \frac{E_a}{kT} J_{dc} $$

  – Typical limits: $J_{dc} < 1 - 2$ mA / $\mu$m²
Self-Heating

- Current through wire resistance generates heat
  - Oxide surrounding wires is a thermal insulator
  - Heat tends to build up in wires
  - Hotter wires are more resistive, slower

- Self-heating limits AC current densities for reliability

\[
I_{\text{rms}} = \sqrt{\frac{1}{T} \int_{0}^{T} I(t) \, dt}
\]

- Typical limits: \( J_{\text{rms}} < 15 \text{ mA/\mu m}^2 \)
Hot Carriers

• Electric fields across channel impart high energies to some carriers
  – These “hot” carriers may be blasted into the gate oxide where they become trapped
  – Accumulation of charge in oxide causes shift in $V_t$ over time
  – Eventually $V_t$ shifts too far for devices to operate correctly

• Choose $V_{DD}$ to achieve reasonable product lifetime
  – Worst problems for inverter and NORs with slow input rise time and long propagation delays
Latchup

- Latchup: positive feedback leading to $V_{DD} - GND$ short
  - Major problem for 1970s CMOS processes before it was well understood
- Avoid by minimizing resistance of body to $GND / V_{DD}$
  - Use plenty of substrate and well taps
Guard Rings

• Latchup risk greatest when diffusion-to-substrate diodes could become forward-biased

• Surround sensitive region with guard ring
Overvoltage

- High voltages can damage transistors
  - Electrostatic discharge (ESD)
  - Oxide arcing
  - Punchthrough
  - Time-dependent dielectric breakdown (TDDB)
    - Accumulated wear from tunneling currents

- Requires low $V_{DD}$ for thin oxides and short channels

- Use ESD protection structures where chip meets real world
Soft Errors

• In 1970s, DRAMs were observed to occasionally flip bits for no apparent reason
  – Ultimately linked to alpha particles and cosmic rays
• Collisions with particles create electron-hole pairs in substrate
  – These carriers are collected on dynamic nodes, disturbing the voltage
• Minimize soft errors by having plenty of charge on dynamic nodes
• Tolerate errors through ECC, redundancy
Summary

• Static CMOS gates are very robust
  – Will settle to correct value if you wait long enough

• Other circuits suffer from a variety of pitfalls
  – Tradeoff between performance & robustness

• Very important to check circuits for pitfalls
  – For large chips, you need an automatic checker
  – Design rules aren’t worth the paper they are printed on unless you back them up with a tool