13. Design Styles and Floorplanning

• This module
  – Custom and semi-custom design
  – Array-based implementations
Design Flow

- Concept
- Architecture
- Logic
- Circuits
- uArchitecture
- Layout
- Si Debug
- Production
- Backend
- Design Execution
- Front End Development
- Technology Readiness
- Silicon Ramp
- Execution
Implementation Choices

Digital Circuit Implementation Approaches

Custom

Semicustom

Cell-based

- Standard Cells
- Compiled Cells

Macro Cells

Array-based

- Pre-diffused (Gate Arrays)
- Pre-wired (FPGA's)
The Custom Approach

Intel 4004

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13. Design Styles

Courtesy Intel
Transition to Automation and Regular Structures

Intel 4004 (‘71)
Intel 8080
Intel 8085
Intel 8286
Intel 8486

Courtesy Intel

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13. Design Styles 5
Cell-based Design (or standard cells)

Routing channel requirements are reduced by presence of more interconnect layers.
Standard Cell — Example

[Brodersen92]
Standard Cell – The New Generation

Cell-structure hidden under interconnect layers
Standard Cell - Example

3-input NAND cell
(from ST Microelectronics):
C = Load capacitance
T = input rise/fall time

<table>
<thead>
<tr>
<th>Path</th>
<th>1.2V - 125°C</th>
<th>1.6V - 40°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>In1—(t_{PLH})</td>
<td>0.073+7.98C+0.317T</td>
<td>0.020+2.73C+0.253T</td>
</tr>
<tr>
<td>In1—(t_{PHL})</td>
<td>0.069+8.43C+0.364T</td>
<td>0.018+2.14C+0.292T</td>
</tr>
<tr>
<td>In2—(t_{PLH})</td>
<td>0.101+7.97C+0.318T</td>
<td>0.026+2.38C+0.255T</td>
</tr>
<tr>
<td>In2—(t_{PHL})</td>
<td>0.097+8.42C+0.325T</td>
<td>0.023+2.14C+0.269T</td>
</tr>
<tr>
<td>In3—(t_{PLH})</td>
<td>0.120+8.00C+0.318T</td>
<td>0.031+2.37C+0.258T</td>
</tr>
<tr>
<td>In3—(t_{PHL})</td>
<td>0.110+8.41C+0.280T</td>
<td>0.027+2.15C+0.223T</td>
</tr>
</tbody>
</table>
Automatic Cell Generation

Initial transistor geometries
Placed transistors
Routed cell
Compacted cell
Finished cell

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13. Design Styles 10
MacroModules

256x32 (or 8192 bit) SRAM
Generated by hard-macro module generator
“Soft” MacroModules

```c
string mat = "booth";
directive (multtype = mat);
output signed [16] Z = A * B;
```

Synopsys DesignCompiler
“Intellectual Property” (IP) Cores

A Protocol Processor for Wireless

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Semicustom Design Flow

Design Iteration

Pre-Layout Simulation -> HDL
Logic Synthesis
Floorplanning
Placement
Routing
Post-Layout Simulation
Circuit Extraction

Design Capture

Behavioral
Structural
Physical
Tape-out

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The “Design Closure” Problem

Iterative Removal of Timing Violations (white lines)

Courtesy Synopsys

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Integrating Synthesis with Physical Design

RTL (Timing) Constraints

Physical Synthesis

Macromodules
Fixed netlists

Place-and-Route Optimization

Netlist with Place-and-Route Info

Artwork

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Design Flow

- Concept
  - Architecture
    - uArchitecture
      - Logic
        - Circuits
          - Layout
            - Si Debug
              - Production

- Technology Readiness
- Front End Development
- Backend
- Design Execution
- Silicon Ramp
This course

• VLSI and Circuit design principles
• HDL design and implementation
• Compiler implementation
• Prototyping and bringup
• FPGA prototyping – omitted 😞