

Karthikeyan Sankaralingam

CONTACT INFORMATION	1210 W. Dayton Street Department of Computer Sciences University of Wisconsin-Madison Madison, WI, 53706 USA	<i>Voice:</i> (608) 890-0121 <i>Fax:</i> (608) 262-9777 <i>E-mail:</i> karu@cs.wisc.edu <i>WWW:</i> www.cs.wisc.edu/~karu
RESEARCH INTERESTS	High-performance computer architecture, microarchitecture, VLSI, and compilers.	
EDUCATION	PhD, Computer Science, December 2006 The University of Texas at Austin Dissertation: "Polymorphous Architectures - A Unified Approach for Extracting Concurrency of Different Granularities" Advisor: Stephen W. Keckler MS, Computer Science, August 2006 The University of Texas at Austin Bachelor of Technology, Indian Institute of Technology, Madras, May 1999	
WORK EXPERIENCE	April '17 - present CEO/CTO & Founder, SimpleMachines Inc. Aug '17 - present Professor, Dept. of Computer Science, University of Wisconsin-Madison. July '13 - July '17 Associate Professor, Dept. of Computer Science, University of Wisconsin-Madison. July '14 - Dec '14 Visiting Professor at Qualcomm (on Sabbatical leave) Dec '06 - June '13 Assistant Professor, Dept. of Computer Science, University of Wisconsin-Madison. Aug '99 - Dec '06 Research Assistant, The University of Texas at Austin, with Prof. Stephen W. Keckler and Prof. Douglas C. Burger in the CART Lab. Jan '03 - May '03 Teaching Assistant, Dept. of Computer Sciences, The University of Texas at Austin. Computer Organization and Programming (Spring 2003), instructor Prof. Stephen W. Keckler. Jun '00 - Aug '00 Internship, IBM Austin Research Lab.	
HONORS AND AWARDS	<ol style="list-style-type: none">1. Vilas Faculty Early Career Investigator Award, 20182. IEEE Micro "Top Picks in Computer Architecture" Award - 2016 (one of twelve).3. IEEE Micro "Top Picks in Computer Architecture" Award - 2015 (two of twelve); One Honorable Mention.	

4. Best of Computer Architecture Letters - 2015 (one of four).
5. Google Faculty Research Award, 2015
6. Emil H. Steiger UW Distinguished Teaching Award, 2014.
7. Philip R. Certain - Gary Sandefur Distinguished Faculty Award, 2013.
8. PLDI Distinguished Paper Award, 2013.
9. IEEE TCCA Young Computer Architect Award, 2012.
10. NSF CAREER Award, 2009.
11. IEEE Micro "Top Picks in Computer Architecture" Award - 2012 (one of twelve).
12. IEEE Micro "Top Picks in Computer Architecture" Award - 2003 (one of fifteen).
13. James C. Browne Fellowship 2004-2005, Department of Computer Sciences, The University of Texas at Austin.
14. Outstanding Research Assistant in the Department of Computer Sciences, in the annual competition for Outstanding Graduate Student Employee, 2003, The University of Texas at Austin.
15. Robert P. Hamilton Best Research Paper Award for "A Design Space Evaluation of Grid Processor Architectures," University Cooperative Society, 2002, The University of Texas at Austin.
16. Best Student Presentation Award, 34th International Symposium on Microarchitecture (MICRO), December 2001, "A Design Space Evaluation of Grid Processor Architectures."

PATENTS

1. **Karthikeyan Sankaralingam**, Tony Nowatzki, and Vinay Gangadhar. "High-Speed Accelerator with Pre-programmed Functions." US patent application filed.
2. **Karthikeyan Sankaralingam**, Tony Nowatzki, and Vinay Gangadhar. "Reconfigurable, Application-Specific Computer Accelerator." US patent application filed.
3. **Karthikeyan Sankaralingam**, Tony Nowatzki, and Vinay Gangadhar. "Computer Architecture with Synergistic Heterogeneous Processors." US patent application filed.
4. **Karthikeyan Sankaralingam**, Newsha Ardalani, and Urmish Thakker. "Method of Estimating Program Speedup in Highly Parallel Applications with Static Analysis." US patent application filed.
5. Tony Nowatzki, Vinay Gangadhar, and **Karthikeyan Sankaralingam**. "Computer with Hybrid Von-Neumann/Dataflow Execution Architecture." US Patent application filed.
6. **Karthikeyan Sankaralingam** and Gregory Wright. "Configuring Coarse-Grained Reconfigurable Arrays (CGRAs) For Dataflow Instruction Block Execution In Block-Based Dataflow Instruction Set Architectures (ISAs)." US Patent application filed.
7. Chen-Han Ho, **Karthikeyan Sankaralingam**, Sung Jin Kim. "Computer Accelerator System with Improved Efficiency." US Patent application filed.
8. **Karthikeyan Sankaralingam**, Jaikrishnan Menon, and Lorenzo De Carli. "Memory Processing Core Architecture." US Patent application filed.
9. **Karthikeyan Sankaralingam**, Newsha Ardalani, and Xiaojin Zhu. "Method of Estimating Program Speedup with Highly Parallel Applications." US patent #9384016.
10. Amir Yazdanbaksh, Raghuraman Balasubramanian and **Karthikeyan Sankaralingam**. "Computer System Predicting Memory Failure." US patent #9384858.

11. Raghuraman Balasubramanian and **Karthikeyan Sankaralingam**. “Integrated Circuit Providing Fault Prediction.” US patent #9500705
12. Jaikrishnan Menon, Marc de Kruijf, and **Karthikeyan Sankaralingam**. “Computer processor providing exception handling with reduced state storage.” US patent #9298497
13. **Karthikeyan Sankaralingam**, Marc de Kruijf, and Chen-Han Ho. “Computer processor providing error recovery with idempotent regions.” US patent #9244772
14. **Karthikeyan Sankaralingam**, Eric Harris, and Samuel Wasmundt. “Lookup engine with reconfigurable low latency computational tiles.” US patent #9231865
15. Cristian Estan and **Karthikeyan Sankaralingam**. “Lookup engine with programmable memory topology.” US patent #7940755.
16. Douglas C. Burger, Stephen W. Keckler, Robert McDonald, Paul Gratz, Nitya Ranganathan, Lakshminarasimhan Sethumadhavan, **Karthikeyan Sankaralingam**, Ramadass Nagarajan, Changkyu Kim, and Haiming Liu. “Dynamically composing processor cores to form logical processors.” US Patent #8180997.
17. Douglas C. Burger, Stephen W. Keckler, **Karthikeyan Sankaralingam**, and Ramadass Nagarajan. “Computing nodes for executing groups of instructions.” US Patent #8055881.
18. Tom Keller and **Karthikeyan Sankaralingam**. “Method and system for enhanced cache efficiency utilizing selective replacement exemption.” US Patent #6772199.

PROFESSIONAL
ACTIVITIES AND
SERVICE

Program Committee: ISCA 2018, ASPLOS 2018, HPCA 2018, MICRO 2017, ISCA 2017, HPCA 2016, IEEE Micro Top-Picks 2016, ISCA 2016, HPCA 2016, MICRO 2015, IEEE Micro Top-Picks 2015, ISCA 2015, HPCA 2014, MICRO 2013, ISCA 2013, NDCA 2011, DSN 2011, MICRO 2010, ISPASS 2009, MICRO 2009, MICRO 2008

Associate Editor: IEEE Computer Architecture Letters

External Program Committee: ASPLOS 2012, ASPLOS 2011, ISCA 2009

Workshop Program Committee: DaSI-2012, UCAS-2010, LCA GPGPU Workshop 2009, CMP-MSI Workshop 2008

Organizing Committee: Finance chair ISCA 2009, Paper Submissions Chair Micro 2007

Conference Reviewer: PACT 2012, ISCA 2012, ISCA 2011, HPCA 2009, ISCA 2008, ISCA 2007, MICRO 2004, ASPLOS 2004, HPCA 2004, ICS 2004, ISCA 2004, ISCA 2003, ICS 2003, ISCA 2002, MICRO 2001

Journal Reviewer: IEEE Micro, Transactions on Dependable and Secure Computing (TDSC), Transactions on Architecture and Code Optimization (TACO), Transactions on VLSI, Computer Architecture Letters, Journal of Parallel and Distributed Computing

Professional membership: ACM (SIGARCH) and IEEE Senior Member (Computer Society)

External review committees: Multiple National Science Foundation Panels

STUDENTS AND
POST-DOCS

1. William Galliher
2. Shunmiao Xu

Graduated Students

1. Vinay Gangadhar (Phd 2017). First employment: Stealth startup.
2. Vijay Thiruvengadam (Phd 2017). First employment: Stealth startup.
3. Tony Nowatzki (Phd 2016); *Awards: Google Fellowship*. First employment Assistant Professor at UCLA.
4. Newsha Ardalani (PhD 2016). First employment: Baidu.
5. Sung Jin Kim (PhD 2015). First employment: Oracle.
6. Venkatraman Govindaraju (PhD 2014); *Awards: Best Student Presentation Award MICRO 2008*. First employment: Oracle.
7. Chen-Han Ho (PhD 2014). First employment: Qualcomm.
8. Emily Blem (PhD 2013). First employment: Google Madison. *Awards: UW-CS Cisco Fellowship, 2012*
9. Marc de Kruijf (PhD 2012). First employment: Google Madison. *Awards: Google Fellowship 2011, 2nd place Cell Programming contest 2007.*
10. Raghuraman Balasubramanian (Masters student). First employment: Google.
11. Jaikrishnan Menon (Masters student). First employment: Intel.
12. Chris Frericks (Masters student). First employment: Samsung.
13. Zach Marzec (Masters student). First employment: Qualcomm.
14. Ryan Cofell (Masters student).
15. Eric Harris (Masters student). First employment: Samsung.
16. Samuel Wasmundt. First employment: Intel.
17. Jesse Benson (joint Bachelors/Masters student). First employment: Microsoft.
18. Matthew D. Sinclair (joint Bachelors/Masters student). PhD Student at UIUC. *Awards: Tre-wartha Undergraduate Honors Research Grant 2008.*
19. Amit Kumar (Masters student). First employment: Intel.
20. Matt Doran (Undergraduate student) *Astronaut Scholarship Foundation ward 2013-2014*
21. Zach York (Undergraduate student)
22. Garret Staus (Undergraduate student). First employment: Intel.
23. Shuou Nomura (industry visitor from Toshiba Design Center).

1. Tony Nowatzki, Vinay Gangadhar, Newsha Ardalani, and Karthikeyan Sankaralingam. “Stream-Dataflow Acceleration.” In Proceedings of the International Symposium on Computer Architecture (**ISCA**), 2017.
2. Tony Nowatzki, Vinay Gangadhar, Greg Wright and Karthikeyan Sankaralingam. “Pushing the Limits of Accelerator Efficiency While Retaining Programmability.” In Proceedings of the International Conference on High Performance Computer Architecture (**HPCA**), 2016. Acceptance Rate: 53/240 (22%).
3. Tony Nowatzki and Karthikeyan Sankaralingam. “Analyzing Behavior Specialized Acceleration.” In Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2016. Acceptance Rate: 53/240 (22%).
4. Raghuraman Balasubramanian, Vinay Gangadhar, Ziliang Guo, Chen-Han Ho, Cherin Joseph, Jaikrishnan Menon, Mario Paulo Drumond, Robin Paul, Sharath Prasad, Pradip Valathol, and Karthikeyan Sankaralingam. “Enabling GPGPU Low-Level Hardware Explorations with MIAOW: An Open-Source RTL Implementation of a GPGPU.” Proceedings of the International Symposium on High Performance and Embedded Architecture and Compilation **HiPEAC**, 2016.
5. Newsha Ardalani, Clint Lestourgeon, **Karthikeyan Sankaralingam**, and Xiaojin Zhu. “Cross-Architecture Performance Prediction (XAPP) Using CPU Code to Predict GPU Performance.” In Proceedings of the International Symposium on Microarchitecture (**MICRO**), 2015. Acceptance Rate: 21% (61/283). [Top Picks Honorable Mention].
6. Raghuraman Balasubramanian, Vinay Gangadhar, Ziliang Guo, Chen-Han Ho, Cherin Joseph, Jaikrishnan Menon, Mario Paulo Drumond, Robin Paul, Sharath Prasad, Pradip Valathol, and Karthikeyan Sankaralingam. “MIAOW - An Open Source GPGPU.” **HOTCHIPS** 27. 2015.
7. Chen-Han Ho, Sung Jin Kim, and **Karthikeyan Sankaralingam**. “Efficient Execution of Memory Access Phases Using Dataflow Specialization.” In Proceedings of the International Symposium on Computer Architecture (**ISCA**), 2015. Acceptance Rate: 19% (58/305).
8. Tony Nowatzki, Vinay Gangadhar, and **Karthikeyan Sankaralingam**. “Exploring the Potential of Heterogeneous Von Neumann/Dataflow Execution Models.” In Proceedings of the International Symposium on Computer Architecture (**ISCA**), 2015. Acceptance Rate: 19% (58/305).
9. Raghuraman Balasubramanian, Vinay Gangadhar, Ziliang Guo, Chen-Han Ho, Cherin Joseph, Jaikrishnan Menon, Mario Paulo Drumond, Robin Paul, Sharath Prasad, Pradip Valathol, and Karthikeyan Sankaralingam. “MIAOW - An Open Source RTL Implementation of a GPGPU.” **COOL Chips XVIII: Proceedings of the International Symposium on Low-Power and High-Speed Chips**, 2015.
10. Chen-Han Ho, Venkatraman Govindaraju, Tony Nowatzki, Ranjini Nagaraju, Zachary Marzec, Preeti Agarwal, Chris Frericks, Ryan Cofell, and Karthikeyan Sankaralingam. “Performance Evaluation of a DySER FPGA Prototype System Spanning the Compiler, Microarchitecture, and Hardware Implementation.” In Proceedings of the International Symposium on Performance Analysis of Systems and Software (**ISPASS**), 2015. Acceptance Rate: 32% (30/92).
11. Raghuraman Balasubramanian, Zach York, Matt Doran, Ari Biswas, Timur Girgin and **Karthikeyan Sankaralingam**. “Hands-on Introduction to Computer Science at the Freshman Level.” In Proceedings of the International Conference on Computer Science Education (**SIGCSE**), 2014. Acceptance Rate: 108/274 (39%).

12. Raghuraman Balasubramanian and **Karthikeyan Sankaralingam**. “Understanding the Impact of Gate-Level Physical Reliability Effects on Whole Program Execution.” In Proceedings of the International Conference on High Performance Computer Architecture (**HPCA**), 2014. Acceptance Rate: 55/215 (26%).
13. Raghuraman Balasubramanian and **Karthikeyan Sankaralingam**. “Virtually-Aged Sampling DMR: Unifying Circuit Failure Prediction and Circuit Failure Detection.” In Proceedings of the International Symposium on Microarchitecture (**MICRO**), 2013. Acceptance Rate: 16% (39/239).
14. Venkatraman Govindaraju, Tony Nowatzki, and **Karthikeyan Sankaralingam**. “Breaking SIMD Shackles: Liberating Accelerators by Exposing Flexible Microarchitectural Mechanisms.” In Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (**PACT**), 2013. Acceptance Rate: 36/208 (17%).
15. Tony Nowatzki, Michael Sartin-Tarm, Lorenzo De Carli, **Karthikeyan Sankaralingam**, Cristian Estan, and Behnam Robotmili. “A General Constraint-centric Scheduling Framework for Spatial Architectures.” In Proceedings of the International Conference on Programming Language Design and Implementation (**PLDI**), 2013.
16. Emily Blem, Jaikrishnan Menon, and **Karthikeyan Sankaralingam**. “Power Struggles: Revisiting the RISC vs. CISC Debate on Contemporary ARM and x86 Architectures.” In Proceedings of the International Conference on High Performance Computer Architecture (**HPCA**), 2013. Acceptance Rate: 51/249 (20%).
17. Wei Zhang, Marc de Kruijf, Ang Li, Shan Lu, and **Karthikeyan Sankaralingam**. “ConAir: Featherweight Concurrency Bug Recovery Via Single-Threaded Idempotent Execution.” In Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2013. Acceptance Rate: 44/191 (23%).
18. Marc de Kruijf and **Karthikeyan Sankaralingam**. “Idempotent Code Generation: Implementation, Analysis, and Evaluation.” In Proceedings of the International Symposium on Code Generation and Optimization (**CGO**), 2013. Acceptance Rate: 33/117 (28%).
19. Chen-Han Ho, Marc de Kruijf, **Karthikeyan Sankaralingam**, Barry Rountree, Martin Schulz, and Bronis R. de Supinski. “Mechanisms and Evaluation of Cross-Layer Fault-Tolerance for Supercomputing.” In Proceedings of the International Conference on Parallel Processing (**ICPP**), 2012. Acceptance Rate: 28% (53/187).
20. Jaikrishnan Menon, Marc de Kruijf, and **Karthikeyan Sankaralingam**. “iGPU: Precise Exception and Speculative Execution on GPUs.” International Symposium on Computer Architecture (**ISCA**), 2012. Acceptance Rate: 18% (47/262).
21. Marc de Kruijf, **Karthikeyan Sankaralingam**, and Somesh Jha. “Static Analysis and Compiler Design for Idempotent Processing.” In Proceedings of the International Conference on Programming Language Design and Implementation (**PLDI**), 2012. Acceptance Rate: 19% (48/255).
22. Jesse Benson, Ryan Cofell, Chris Frericks, Venkatraman Govindaraju, Chen-Han Ho, Tony Nowatzki, and **Karthikeyan Sankaralingam**. “Design Integration and Implementation of the DySER Hardware Accelerator into OpenSPARC.” In Proceedings of the International Conference on High Performance Computer Architecture (**HPCA**), 2012. Acceptance Rate: 17% (36/210).

23. Marc de Kruijf and **Karthikeyan Sankaralingam**. “Idempotent Processor Architecture.” In Proceedings of the International Symposium on Microarchitecture (**MICRO**), 2011. Acceptance Rate: 21% (44/209).
24. Nilay Vaish, Thawan Kooburat, Lorenzo de Carli, **Karthikeyan Sankaralingam**, and Cristian Estan, “Experiences in Co-designing a Packet Classification Algorithm and a Flexible Hardware Platform.” In Proceedings of the International Symposium on Architectures for Networking and communication Systems (**ANCS**), 2011. Acceptance Rate: 32% (20/62).
25. Hadi Esmailzadeh, Emily Blem, Renée St. Amant, **Karthikeyan Sankaralingam**, and Doug Burger, “Dark Silicon and the End of Multicore Scaling.” In Proceedings of the International Symposium on Computer Architecture (**ISCA**), 2011. Acceptance Rate: 19% (40/208).
26. Shuou Nomura, Matthew D. Sinclair, Chen-Han Ho, Venkatraman Govindaraju, Marc de Kruijf, and **Karthikeyan Sankaralingam**, “Sampling + DMR: Practical and Low-overhead Permanent Fault Detection.” In Proceedings of the International Symposium on Computer Architecture (**ISCA**), 2011. Acceptance Rate: 19% (40/208).
27. Venkatraman Govindaraju, Chen-Han Ho, and **Karthikeyan Sankaralingam**, “Dynamically Specialized Datapaths for Energy Efficient Computing.” In Proceedings of the International Conference of High-Performance Computer Architecture (**HPCA**), 2011. Acceptance Rate: 19% (42/227).
28. Shuou Nomura, **Karthikeyan Sankaralingam**, and Ranganathan Sankaralingam, “A Fast and Highly Accurate Path Delay Emulation Framework for Logic-Emulation of Timing Speculation.” In Proceedings of the International Test Conference (**ITC**), 2010. Acceptance Rate: 34% (81/239).
29. Amit Kumar, Lorenzo De Carli, Sung Jin Kim, Marc de Kruijf, **Karthikeyan Sankaralingam**, Cristian Estan, and Somesh Jha. “Design and Implementation of the PLUG Architecture for Programmable and Efficient Network Lookups.” In Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (**PACT**), 2010. Acceptance Rate: 46/266 (18%).
30. Marc de Kruijf, Shuou Nomura, and **Karthikeyan Sankaralingam**. “Relax: An Architectural Framework for Software Recovery of Hardware Faults.” In Proceedings of the International Symposium on Computer Architecture (**ISCA**), 2010. Acceptance Rate: 18% (44/245).
31. Marc de Kruijf, Shuou Nomura, and **Karthikeyan Sankaralingam**. “A Unified Model for Timing Speculation: Evaluating the Impact of Technology Scaling, CMOS Design Style, and Fault Recovery Mechanism.” In Proceedings of the International Conference on Dependable Systems and Networks (**DSN**), 2010. Acceptance Rate: 25% (26/104).
32. Lorenzo De Carli, Yi Pan, Amit Kumar, Cristian Estan, and **Karthikeyan Sankaralingam**. “PLUG: Flexible Lookup Modules for Rapid Deployment of New Protocols in High-speed Routers.” In SIGCOMM, 2009. Acceptance Rate: 10% (27/270).
33. Randy Smith, Neelam Goyal, Justin Ormont, **Karthikeyan Sankaralingam**, and Cristian Estan. “Evaluating GPUs for Network Packet Signature Matching.” In Proceedings of the International Symposium on Performance Analysis of Systems and Software (**ISPASS**), 2009. Acceptance Rate: 28% (24/86).
34. Venkatraman Govindaraju, Peter Djeu, **Karthikeyan Sankaralingam**, Mary Vernon, and William R. Mark. “Toward a Multicore Architecture for Real-time Ray-tracing.” In Proceedings of the

- International Symposium on Microarchitecture (**MICRO**), 2008. [Best student presentation Venkatraman Govindaraju]. Acceptance Rate: 19% (40/210).
35. Daniel Sanchez, Luke Yen, Mark D. Hill, and **Karthikeyan Sankaralingam**. “Implementing Signatures for Transactional Memory.” In Proceedings of the International Symposium on Microarchitecture (**MICRO**), 2007. Acceptance Rate: 21% (35/166).
 36. Madhu Sibi Govindan, **Karthikeyan Sankaralingam**, Ramdas Nagarajan, Robert McDonald, Rajagopalan Desikan, Saurabh Drolia, Paul Gratz, Divya Gulati, Heather Hanson, Changkyu Kim, Haiming Liu, Nitya Ranganathan, Simha Sethumadhavan, Sadia Sharif, Premkishore Shivakumar, Stephen W. Keckler, and Doug Burger. “TRIPS: A Distributed Explicit Data Graph Execution (EDGE) Microprocessor.” HotChips 19, 2007.
 37. Paul Gratz, **Karthikeyan Sankaralingam**, Heather Hanson, Premkishore Shivakumar, Robert McDonald, Stephen W. Keckler, and Doug Burger. “Implementation and Evaluation of a Dynamically Routed Processor Operand Network. In Proceedings of the 1st ACM/IEEE International Symposium on Networks-on-Chip (**NOCS**), 2007.
 38. **Karthikeyan Sankaralingam**, Ramdas Nagarajan, Robert McDonald, Rajagopalan Desikan, Saurabh Drolia, M.S. Govindan, Paul Gratz, Divya Gulati, Heather Hanson, Changkyu Kim, Haiming Liu, Nitya Ranganathan, Simha Sethumadhavan, Sadia Sharif, Premkishore Shivakumar, Stephen W. Keckler, and Doug Burger. “Distributed Microarchitectural Protocols in the TRIPS Prototype Processor.” In Proceedings of the International Symposium on Microarchitecture (**MICRO**), 2006. Acceptance Rate: 24% (42/174).
 39. Aaron Smith, Ramdas Nagarajan, **Karthikeyan Sankaralingam**, Robert McDonald, Doug Burger, Stephen W. Keckler, Kathryn S. McKinley. “Dataflow Predication.” In Proceedings of the International Symposium on Microarchitecture (**MICRO**), 2006. Acceptance Rate: 24% (42/174).
 40. **Karthikeyan Sankaralingam**, Stephen W. Keckler, William R. Mark, and Doug Burger. “Universal Mechanisms for Data Parallel Architectures.” In Proceedings of the International Symposium on Microarchitecture (**MICRO**), 2003. Acceptance Rate: 25% (34/135).
 41. **Karthikeyan Sankaralingam**, Vincent A. Singh, Stephen W. Keckler, and Doug Burger. “Routed Inter-ALU Networks for ILP Scalability and Performance.” In Proceedings of the International Conference on Computer Design (**ICCD**), 2003. Acceptance Rate: 26% (77/296).
 42. **Karthikeyan Sankaralingam**, Ramdas Nagarajan, Haiming Liu, Changkyu Kim, Jaehyuk Huh, Doug Burger, Stephen W. Keckler, and Charles R. Moore. “Exploiting ILP, TLP and DLP with the Polymorphous TRIPS Architecture.” In Proceedings of the International Symposium on Computer Architecture (**ISCA**), 2003. Acceptance Rate: 20% (36/184).
 43. **Karthikeyan Sankaralingam**, Simha Sethumadhavan, and James C. Browne. “Distributed Pagerank for P2P Systems.” In Proceedings of the International Symposium on High Performance Distributed Computing (**HPDC**), June 2003. Acceptance Rate: 25% (25/125).
 44. Stephen W. Keckler, Doug Burger, Charles R. Moore, Ramdas Nagarajan, **Karthikeyan Sankaralingam**, Vikas Agarwal, M.S. Hrishikesh, Nitya Ranganathan, and Premkishore Shivakumar. “A Wire-Delay Scalable Microprocessor Architecture for High Performance Systems.” In Proceedings of the International Solid-State Circuits Conference (**ISSCC**), 2003. Acceptance Rate: 43.5% (157/360).
 45. Ramdas Nagarajan, **Karthikeyan Sankaralingam**, Doug Burger, and Stephen W. Keckler. “A Design Space Evaluation of Grid Processor Architectures.” In Proceedings of the International

Symposium on Microarchitecture (**MICRO**), 2001. [Best Student Presentation Award]. Acceptance Rate: 20% (29/144).

46. **Karthikeyan Sankaralingam** and S.R. Chakravarthy. “Computer Model of Flamelet Distribution on the Burner Surface of Composite Solid Propellants.” In Proceedings of the 38th Aerospace Sciences Meeting Conference and Exhibit, 2000.
47. **Karthikeyan Sankaralingam** and Ranganathan Sankaralingam. “More on Arbitrary Boundary Packed Arithmetic.” In Proceedings of the International Conference on High Performance Computing (**HiPC**), 1998.

REFEREED JOURNAL PUBLICATIONS

48. Gagan Gupta, Tony Nowatzki, Vinay Gangadhar, and Karthikeyan Sankaralingam. “Kickstarting Semiconductor Innovation with Open Source Hardware.” *IEEE Computer*, 50, 2017.
49. Tony Nowatzki, Vinay Gangadhar, Greg Wright, and Karthikeyan Sankaralingam. “Domain Specialization Is Generally Unnecessary for Accelerators.” *IEEE Micro (Top Picks Issue)*, 37, 2017.
50. **Karthikeyan Sankaralingam** and Cristian Estan. “Memory Processing Units.” *IEEE Micro (Position paper)* 2016.
51. Chen-Han Ho, Sung Jin Kim, and **Karthikeyan Sankaralingam**. “Accelerating the Accelerator Memory Interface with Access-Execute and Dataflow.” *IEEE Micro Top Picks Special Issue*, 2016.
52. Tony Nowatzki, Vinay Gangadhar, and **Karthikeyan Sankaralingam**. “A Heterogeneous Von Neumann/Explicit Dataflow Processor.” *IEEE Micro Top Picks Special Issue*, 2016.
53. Tony Nowatzki, Venkatraman Govindaraju, and **Karthikeyan Sankaralingam**. “A Graph-Based Program Representation for Analyzing Hardware Specialization Approaches.” *Computer Architecture Letters*, August 2015. **Best of CAL Award**.
54. Raghuraman Balasubramanian, Vinay Gangadhar, Ziliang Guo, Chen-Han Ho, Cherin Joseph, Jaikrishnan Menon, Mario Paulo Drumond, Robin Paul, Sharath Prasad, Pradip Valathol, and **Karthikeyan Sankaralingam**. “Enabling GPGPU Low-level Hardware Explorations with MIAOW - An Open Source RTL Implementation of a GPGPU.” *ACM Transactions on Architecture and Code Optimization*, 2015.
55. Tony Nowatzki, Jaikrishnan Menon, Chen-Han Ho, and **Karthikeyan Sankaralingam**. “Architectural Simulators Considered Harmful.” *IEEE Micro*, 2015.
56. Amir Yazdanbakhsh, Raghuraman Balasubramanian, Tony Nowatzki, and **Karthikeyan Sankaralingam**. “Comprehensive Circuit Failure Prediction and Detection for Logic and SRAM using Virtual Aging, Sampled Redundancy, and Asymmetric Checkers.” *IEEE Micro*, 2015.
57. Emily Blem, Jaikrishnan Menon, and Vijayaraghavan Thiruvengadam and **Karthikeyan Sankaralingam**. “ISA Wars: Understanding the Relevance of ISA being RISC or CISC to Performance, Power and Energy on Modern Architectures.” *ACM Transactions on Computer Systems (TOCS)*, 2015.
58. Tony Nowatzki, Michael Sartin-Tarm, Lorendo De Carli, **Karthikeyan Sankaralingam**, Cristian Estan, and Behnam Robatmili. “A Scheduling Framework for Spatial Architectures Across Multiple Constraint-solving Theories.” *ACM Transactions on Programming Languages and Systems (TOPLAS)* 2014.

59. Michael Sartin-Tarm, Tony Nowatzki, Lorenzo De Carli, **Karthikeyan Sankaralingam**, and Cristian Estan. "Constraint centric scheduling guide." SIGARCH Computer Architecture News, 41(2):17-21, ACM, New York, NY, USA, May 2013.
60. Hadi Esmaeilzadeh, Emily Blem, Rene St. Amant, karu, and Doug Burger. "Power challenges may end the multicore era." Communications of the ACM, 56(2):93-102. 2013.
61. Emily Blem, Hadi Esmaeilzadeh, Renée St. Amant, **Karthikeyan Sankaralingam**, Doug Burger. "Multicore Model from Abstract Single Core Inputs" Computer Architecture Letters, 2012.
62. Venkatraman Govindaraju, Chen-Han Ho, Tony Nowatzki, Jatin Chhugani, Nadathur Satish, **Karthikeyan Sankaralingam**, and Changkyu Kim. "DySER: Unifying Functionality and Parallelism Specialization for Energy Efficient Computing." IEEE Micro, Volume 32, Issue 5. [Special Issue on Energy-Aware Computing]
63. Hadi Esmaeilzadeh, Emily Blem, Rene St. Amant, **Karthikeyan Sankaralingam**, Doug Burger. "How Power Challenges May End the Multicore Revolution" Communications of the ACM, 2012. [Research Highlights Invited Paper]
64. Hadi Esmaeilzadeh, Emily Blem, Rene St. Amant, **Karthikeyan Sankaralingam**, Doug Burger. "Power Limitations and Dark Silicon Challenge the Future of Multicore." ACM Transactions on Computer Systems (TOCS), 2012. [Invited Paper]
65. Hadi Esmaeilzadeh, Emily Blem, Rene St. Amant, **Karthikeyan Sankaralingam**, Doug Burger. "Dark Silicon and the End of Multicore Scaling." IEEE Micro Top Picks Special Issue, Volume 32, Issue 3, 2012.
66. Chen-Han Ho, Garret Staus, Aaron Ullmer, and **Karthikeyan Sankaralingam**. "Exploring the Interaction Between Device Lifetime Reliability and Security Vulnerabilities." Computer Architecture Letters, 10, 2011.
67. Marc de Kruijf and **Karthikeyan Sankaralingam**. "MapReduce for the CELL B.E. Architecture." IBM Journal of Research and Development, Volume 53, Number 5, 2009. [Invited Paper]
68. Paul Gratz, Changkyu Kim, **Karthikeyan Sankaralingam**, Heather Hanson, Premkumar Shivakumar, Stephen W. Keckler, and Doug Burger. "On-Chip Interconnection Networks of the TRIPS Chip." IEEE Micro, Volume 27, Issue 5, 2007.
69. **Karthikeyan Sankaralingam**, Ramdas Nagarajan, Haiming Liu, Changkyu Kim, Jaehyuk Huh, Nitya Ranganathan, Doug Burger, Stephen W. Keckler, Robert McDonald, and Charles .R. Moore. "TRIPS: A polymorphous architecture for exploiting ILP, TLP, and DLP." ACM Transactions on Architecture and Code Optimization (TACO), Volume 1, Issue 1, 2004. [Invited Paper]
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ABBREVIATIONS

ISCA	International Symposium on Computer Architecture
DSN	Dependable Systems and Networks
NDCA	New Directions in Computer Architecture
MICRO	International Symposium on Microarchitecture
ISPASS	International Symposium on Performance Analysis of Systems and Software
ASPLOS	International Conference on Architectural Support for Programming Languages and Operating Systems
Da-SI	Dark Silicon Workshop
UCAS	Workshop on Unique Chips and Systems
LCA GPGPU	Workshop on Language, Compiler, and Architecture Support for GPGPU
CMP-MSI	Workshop on Chip Multiprocessor Memory Systems and Interconnects
HPCA	International Symposium on High Performance Computer Architecture
ICS	International Conference on Supercomputing