Kevin E. Moore

Department of Computer Sciences
University of Wisconsin–Madison
1210 W. Dayton St.
Madison, WI 53706

Email: kmoore@cs.wisc.edu
Phone: (608) 262-6619
Fax: (608) 262-9777
Home Page: http://www.cs.wisc.edu/~kmoore

RESEARCH INTERESTS

Computer Architecture with a focus on:

- Multiprocessor and chip multiprocessor memory systems
- Transactional memory
- Improving the hardware/software interface to increase parallelism
- Characterization of parallel server workloads

EDUCATION

University of Wisconsin–Madison – Ph. D. Department of Computer Sciences (expected 2006)
Advisor: Prof. David A. Wood

University of Wisconsin–Madison – Master of Sciences, Computer Science, 2001

Duke University – BSE, Electrical and Computer Engineering, 1997

PROFESSIONAL EXPERIENCE

Research Assistant - Wisconsin Multifacet Project, Department of Computer Sciences, University of Wisconsin—Madison (since Spring 2000)

- Member of the Multifacet Project (http://www.cs.wisc.edu/multifacet/) co-directed by Professors Mark D. Hill and David A. Wood
- Designed and evaluated LogTM, an efficient implementation of transactional memory
- Contributed to the Multifacet General Execution-driven Multiprocessor Simulation (GEMS) toolset

Intern - Sun Microsystems Labs (Summer 2001)

- Characterized memory-system and processor behavior of commercial servers running the ECperf (now SPECjAppServer) benchmark

Teaching Assistant - Department of Computer Sciences, University of Wisconsin, Madison (Fall 1999)

- Led two discussion sections for an introductory programming course

Associate Software Engineer - International Research Institute (1997 – 1999)

- Developed command and control software in C++ and Java

SKILLS

Programming

Proficient in Java, C++ and Python. Experience working in small groups and as part of large software engineering project.

C/C++: 1 year full time, 10 years part time

Java: 1 year full time, 4 years part time

Python: 4 years part time

SQL/Perl/Shell scripts: Some familiarity

Modeling and Simulation – 6 years experience developing detailed memory system timing models using Virtutech Simics. Working knowledge of queuing theory-based analytical modeling.

REFEREED CONFERENCE PUBLICATIONS

ISCA-07 Jayaram Bobba, Kevin E. Moore, Haris Volos, Luke Yen, Mark D. Hill, Michael M. Swift and David A. Wood, "Performance Pathologies in Hardware Transactional Memory." *Thirty-Fourth International Symposium on Computer Architecture (ISCA)*, June 2007.

HPCA-07 Luke Yen, Jayaram Bobba, Michael R. Marty, Kevin E. Moore, Haris Volos, Mark D. Hill, Michael M. Swift and David A. Wood, "Decoupling Hardware Transactional Memory from Caches." *Thirteenth International Symposium on High Performance Computer Architecture (HPCA)*, February 2007.

ASPLOS-06 Michelle J. Moravan, Jayaram Bobba, Kevin E. Moore, Luke Yen, Mark D. Hill, Ben Liblit, Michael M. Swift and David A. Wood, "Supporting Nested Transactions in LogTM." *Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.

HPCA-06 Kevin E. Moore, Jayaram Bobba, Michelle J. Moravan, Mark D. Hill and David A. Wood, "LogTM: Log-Based Transactional Memory." *Twelfth International Symposium on High Performance Computer Architecture (HPCA)*, February 2006.

ICPP-05 Martin Karlsson, Kevin E. Moore, Erik Hagersten and David A. Wood, "Exploring Processor Design Options for Java Based Middleware." *2005 International Conference on Parallel Processing (ICPP), June 2005*.

HPCA-03 Martin Karlsson, Kevin E. Moore, Erik Hagersten and David A. Wood, "Memory System Behavior of Java-Based Middleware." *Ninth International Symposium on High Performance Computer Architecture (HPCA)*, February 2003.

ASPLOS-00 Milo M. K. Martin, Daniel J. Sorin, Anastassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson, Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill and David A. Wood, "Timestamp Snooping: An Approach for Extending SMPs." *Ninth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, November 2000.

JOURNAL PUBLICATIONS

COMPUTER Alaa R. Alameldeen, Milo M. K. Martin, Carl J. Mauer, Kevin E. Moore, Min Xu, Daniel J. Sorin, Mark D. Hill and David A. Wood, "Simulating a $2M Commercial Server on a $2K PC." *IEEE Computer*, February 2003.

REFEREED WORKSHOP PUBLICATIONS

WMPI-02 Martin Karlsson, Kevin E. Moore, Erik Hagersten and David A. Wood, "Memory Characterization of the ECperf Benchmark." *Second Annual Workshop on Memory Performance Issues (WMPI)*, in conjunction with ISCA-29, June 2002.

NON-REFEREED PUBLICATIONS

CAN-05 Milo M.K. Martin, Daniel J. Sorin, Bradford M. Beckmann, Michael R. Marty, Min Xu, Alaa R. Alameldeen, Kevin E. Moore, Mark D. Hill, and David A. Wood, "Multifacet's General Execution-driven Multiprocessor Simulator (GEMS) Toolset." *Computer Architecture News (CAN)*, September 2005.

TR1524 Kevin E. Moore, Mark D. Hill and David A. Wood, "Thread-Level Transactional Memory." Univ. of Wisconsin Computer Sciences Technical Report CS-TR-2005-1524, March 2005.

INVITED AND CONFERENCE TALKS

LogTM: Log-Based Transactional Memory:

- 12th International Symposium on High Performance Computer Architecture (HPCA), Austin TX, February 2006
- Invited Talk, Sun Microsystems Labs, Burlington, MA, September, 2006
- Intellectual Dessert Seminar, Sun Microsystems Labs, Menlo Park, CA, August, 2006
- Invited Talk, University of Auckland, Auckland, New Zealand, January 2006
- Invited Talk, Victoria University, Wellington, New Zealand, January 2006
- 9th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, WI, October 2005

Supporting Nested Transactional Memory in LogTM:

- 12th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), San Jose, CA, October 2006
- 10th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, WI, October 2006

Thread-Level Transactional Memory:

- 8th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, WI, October 2004

Memory System Behavior of Java-Based Middleware:

- 9th International Symposium on High Performance Computer Architecture (HPCA), February 2003

PROFESSIONAL ACTIVITIES

- External reviewer for the International Symposium on High Performance Computer Architecture (HPCA) and Science of Computer Programming (SCP)
- Organizer of the weekly Computer Architecture Seminar at the University of Wisconsin–Madison Fall 2004—Spring 2005
- Student Member of the ACM
- Member of ACM Special Interest Group on Computer Architecture (SIGARCH)

REFERENCES

Professor David A. Wood
Department of Computer Sciences
University of Wisconsin-Madison
1210 West Dayton Street
Madison, WI 53706
Email: david@cs.wisc.edu
Phone: 608-263-7463
Department: 608-262-1204
Fax: 608-262-9777

Professor Mark D. Hill
Department of Computer Sciences
University of Wisconsin-Madison
1210 West Dayton Street
Madison, WI 53706
Email: markhill@cs.wisc.edu
Phone: 608-262-2196
Department: 608-262-1204
Fax: 608-262-9777

Professor James R. Goodman
Department of Computer Science
The University of Auckland
Science Center, Level 3
Building 303
38 Princes Street
Auckland, New Zealand
Email: goodman@cs.auckland.ac.nz
Phone: +64 (9) 373-7599 x88752

Additional references available on request.