Introduction

Be sure to print a copy of Experiment #1 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring graph paper (cm × cm is best).

The purpose of this experiment is to get familiar with the function generator and the oscilloscope and to practice making measurements.

During your lab session read very carefully and do everything just as described in the text. For each question that you encounter in the text, write down the question and then answer the question. There is very little calculation required. Please do draw the sketches mentioned in the experiment.

This experiment is a bit long and so you may not finish. That's OK. There will be no penalty if you do not finish. But do as much as you can. It will make the next experiment go easier for you. To prepare for this experiment:

1. Read the entire experiment.
2. Write down all the questions that are asked in the text of the experiment.
3. Prepare a title page, purpose paragraph, no theory or circuit analysis, and the questions (with space for the answers) in advance to coming to lab.

Your report, which is due at the beginning of the next lab session, will include the material above, the answers to the questions (which you will determine from performing the experiment), and a conclusion paragraph. There should be just one report from each lab group.

Purpose

In this experiment, you will display some waveforms on the oscilloscope. In doing so, this should help you become familiar with the pulse generator and oscilloscope, which will be used extensively in this laboratory.

Parts

None

Theory

In ECE 340 and ECE 342, you will use a digital oscilloscope as opposed to the analog scopes that you have used in previous courses. This scope is basically an analog scope with a digital sampling front-end. Figure 1 shows the block diagram.

The analog portion of this scope is the horizontal and vertical deflection amplifier similar to those found in older scopes. These amplifiers move the electron beam horizontally and vertically across the scope screen. Ultimately, the vertical signal is obtained from the "outside" world – i.e. the scope probes. Ultimately, the horizontal signal can be obtained from the "outside" world or from an internal ramp generator.

In a digital scope, the external signals are first sampled, converted to an 8-bit digital word (analog-to-digital conversion), stored in memory, retrieved from memory by a microprocessor, converted

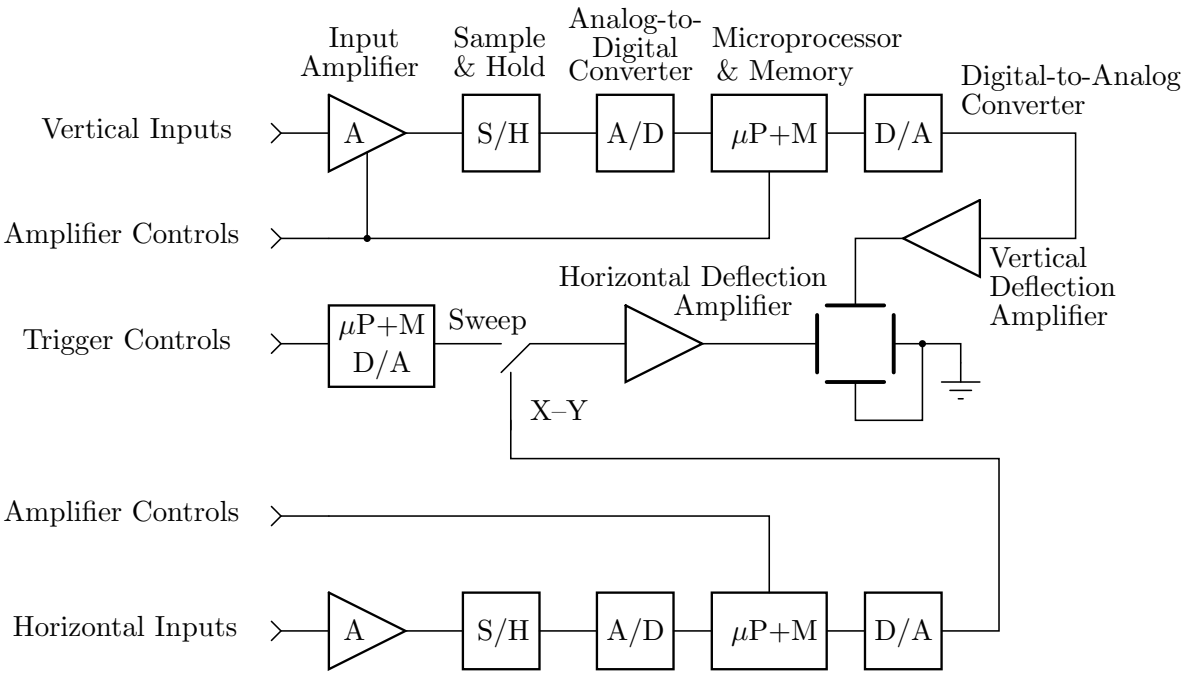

Figure 1:

back to an analog voltage level (digital-to-analog conversion), and finally "fed" to the appropriate deflection amplifiers. At first glance, the conversion of the analog signal to a digital word only to be re-converted to an analog voltage seems needlessly redundant. However, the power of the digital oscilloscope is found in the ability of the microprocessor (really a small computer) to perform some pre-programmed signal processing functions and, thus, display the signal in an intelligible form along with other desired information.

The various signal processing functions are chosen by using a combination of hardwired (hard) keys, push button switches on the front panel to the right of the screen, and software controlled (soft) keys, push button switches below the screen. Each hard key calls up a menu of choices you can make using the soft keys. Figure 2 shows an example of a menu if the MODE hard key is pushed.

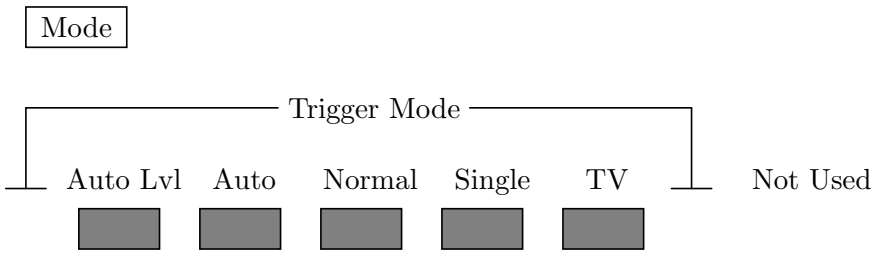

Figure 2:

The laboratory is equipped with an examination copy of the User Guide for this oscilloscope, consult it, or ask your laboratory instructor if you have any questions.

Procedure

1. Make a drawing of the front panel to the right of the screen. On your drawing label all the knobs and hard keys.

2. For each hard key, complete a diagram similar to Figure 2. You should have diagrams for the following hard keys: 1, 2, ±, Main/Delayed, Source, Mode, Slope/Coupling, TV, Print/Utility, Cursors, Display, Setup, Trace, Voltage, and Time. Please note that the last two keys have two menus. The keys grouped under the heading of "Measure"–Voltage, Time and Cursors– will be used most frequently. The following two procedures will allow you the opportunity to experiment with these functions.

3. Connect the pulse generator to the scope using a coaxial cable with each end terminated in a BNC connector. Display the waveform shown in Figure 3 on the scope screen. The waveform shown in Figure 3 is an idealization. In particular, a perfect rectangular (rising and falling edges) waveform cannot be produce by the pulse generator. Use the VOLTAGE key to find Vpp, Vavg, Vrms, Vmax, Vmin, Vtop, and Vbase. Use the TIME key to find Freq(uency), Period, Duty Cy(cle), +Width, −Width, RiseTime, and FallTime.

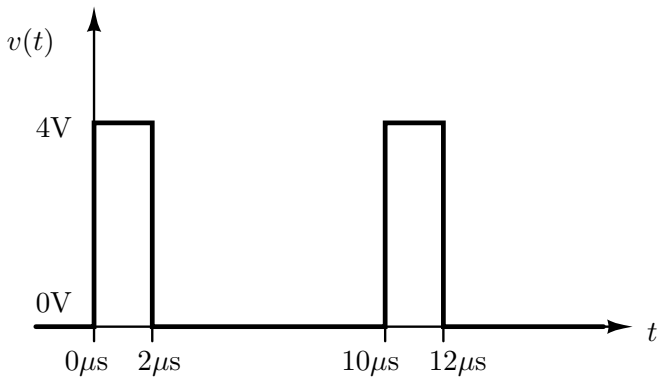

Figure 3:

4. Display the waveform shown in Figure 4. Do the same measurements as you did in Procedure #3.

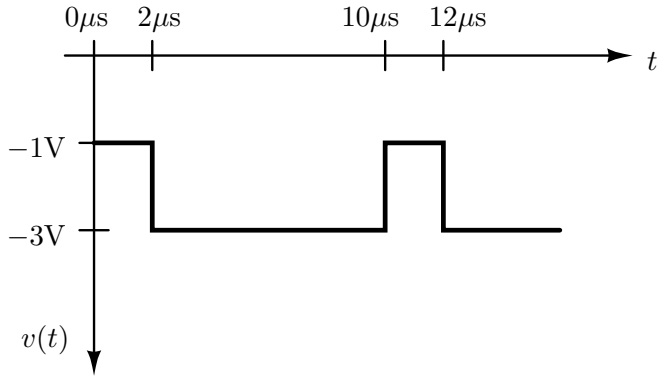

Figure 4:

5. Construct the circuit shown in Figure 5, using a 1 kΩ resistor for R and a 47pF capacitor for C. Set the pulse generator to output the waveform depicted in Figure 3. Use the dual trace capability of the oscilloscope to measure the delay of the RC circuit. We will define the delay as the time from when the input voltage changes until the time when the output wave form has switched halfway from its initial to its final voltage levels. Measure both the low-to-high delay, t_{LH}, and the high-to-low delay, t_{HL}.

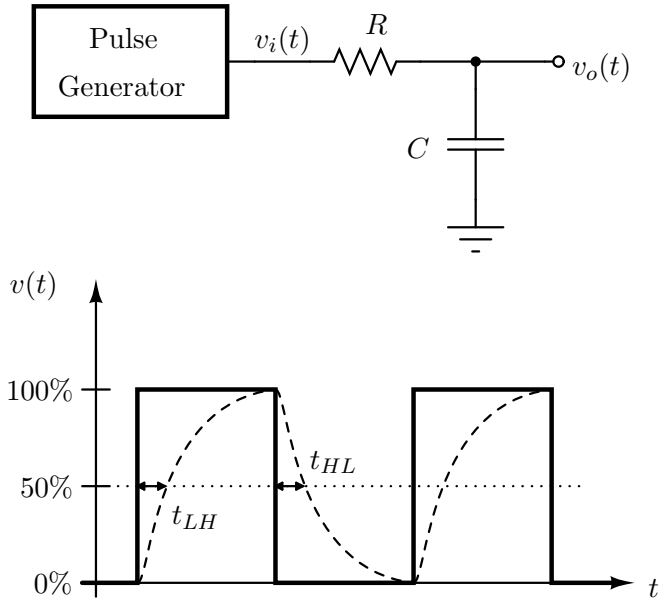

Figure 5:

6. Repeat Procedure 5 with a 10 kΩ resistor and input period of 10 ms. You will have to increase the time between input pulses coming from the pulse generator.

7. Repeat Procedure 5 with the positions of the 1 kΩ resistor and the capacitor exchanged.

Note: When using the pulse generator the Normal/Double switch should be set to Normal, and the Delay sliding switch should be set to zero–the far left.

Questions

1. Calculate the average and RMS voltage levels for the two waveforms for Procedures 3 & 4 and compare them with the measured values.

2. Recall the standard formula for the capacitor voltage during transients in a RC circuit:

$$v(t) = v(t_0) + [v(\infty) - v(t_0)]\left(1 - \exp\left(-\frac{t - t_0}{RC}\right)\right)$$

The equation is valid for $t > t_0$, the time at which the voltage across the series combination of the resistor and capacitor is switched. Calculate the delay times, t_{LH} and t_{HL}, for Procedures 5-7. How do they compare with measured values?

Introduction

Be sure to print a copy of Experiment #2 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring graph paper (cm × cm is best).

Be sure that your lab team purchases a ECE 340 lab kit from the bookstore *before* coming to lab. We do not give out part to students in this lab.

Be sure to read the Lab Policy and know your laboratory responsibilities as outlined in the document "ECE 340 Laboratory Information" posted on the course webpage.

Preliminary Preparation

There is a great deal of preparation required for this experiment! **This work is to to be done before coming to your lab session**. Follow the "Preliminary Questions" section as an outline for your preparation.

Be sure to keep the Power Supply turned **OFF** until you are sure a circuit is constructed correctly. When in lab, work methodically but work quickly so that you will finish before the end of the lab session.

Purpose

To investigate the effect that feedback has on the overall operation of the amplifier and how various mathematical operations may be realized by means of specific types of feedback.

Parts

- 1 - 741 Operational Amplifier
- Assorted Resistors

Theory

An operational amplifier (op-amp) is an analog circuit element that can perform many mathematical operations on the analog input signals. Some of these operations are additions of two signals, multiplication of a signal by a constant, integration of a signal, and differentiation of a signal.

Most of these operational circuits can be understood and analyzed using a simple ideal op-amp model for the "real" op-amp. The following are the characteristics of the ideal op-amp as shown in Figure 1(a):

- The input impedance $Z_{in} = \infty$; therefore, $I_+ = 0$ and $I_- = 0$;
- The open loop gain $A \to \infty$; therefore, terminal voltages $V_+ = V_-$ in order for the output voltage V_o ($V_o = A(V_+ - V_-)$) to remain finite.
- The output impedance $Z_{out} = 0$; therefore, the opamp output voltage is not a function of the load impedance connected to the output.

Circuits with op-amps should be analyzed using the model of Figure 1(b). Nodal analysis should be used to obtain the desired transfer function as a function of A. Further simplifications occur as expressions are subjected to the limit as $A \to \infty$.

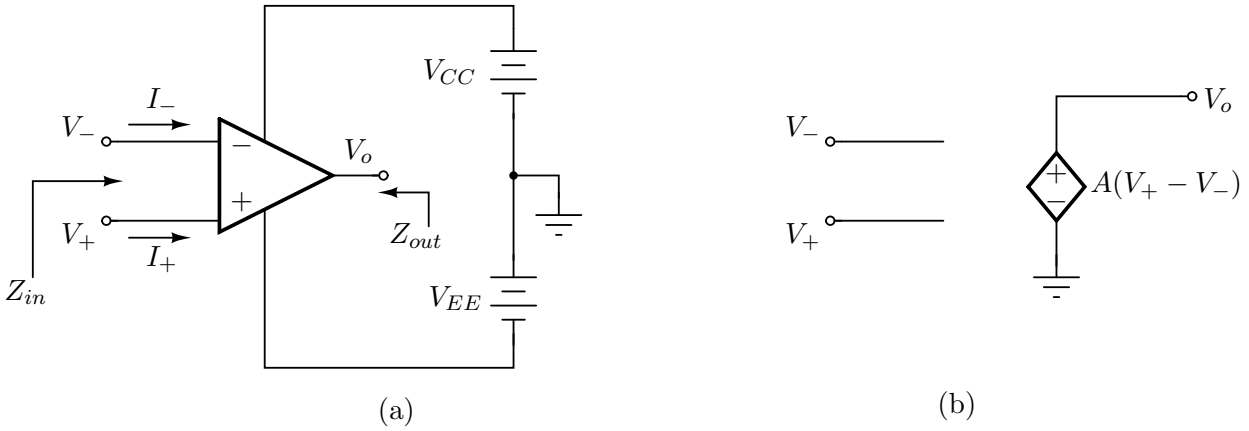

Figure 1:

741 OpAmp Terminals

As with all IC's (integrated circuits) you need to know the purpose of each pin on the 741 op-amp. Hold the IC looking down on the top surface (pins facing away from you). Orient the IC so that the "cut-out" is to the left. Then pin 1 will be in the lower left-hand corner. The pins are numbered 1-8 going around the IC counter-clockwise from pin 1. Here is a list of pins and their purpose:

1. NC (No Connection)
2. Inverting input $V-$
3. Non-inverting input $V+$
4. Negative Power Supply Connection $V_{PS-} = -15$ V.
5. NC
6. Output V_o
7. Positive Power Supply Connection $V_{PS+} = +15$ V.
8. NC

Preliminary Questions

1. Obtain an expression for V_o in terms of V_1, V_2, V_3 and the resistances in Figure 2.
2. Design single input op-amp circuits with with closed loop gains of -10, $+10$, $+1$ and -1. Use 10kΩ for the feedback resistor R_f in your designs. What type of feedback is used in the ± 10 gain amplifiers? Explain with appropriate equations the effect of feedback on input and output resistances of the amplifier circuits.

3. Design two op-amp circuits with input voltages V_x and V_y, for which the output voltage is $V_o = 5(V_x - V_y)$ and $V_o = -5(V_x + V_y)$, respectively.

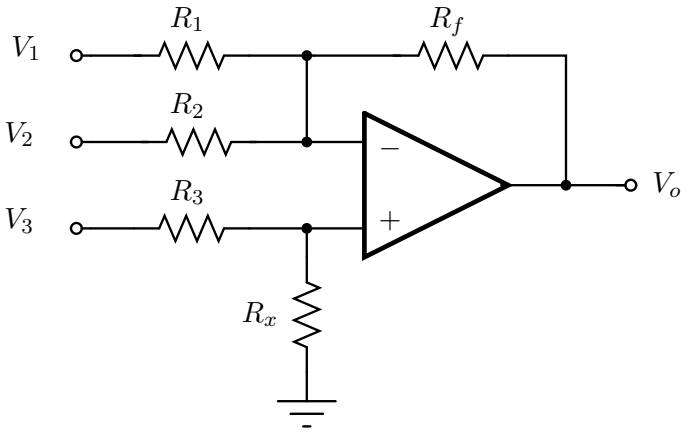

Figure 2:

Procedure

1. As you construct the circuits from preliminary question 2 **be sure to keep the power supply turned OFF until you are sure a particular circuit is constructed correctly**.

2. For the amplifier with a gain of -10,

   (a) Apply a sinusoidal voltage waveform of suitable amplitude to the input of the amplifier (you may need to use a voltage divider to reduce the signal generator voltage), and verify the gain.

   (b) Plot the frequency response from 10 Hz to 100 kHz.

   (c) Increase the amplitude of the input signal and note the effect of saturation. Record the output voltage limits. Sketch the output waveform.

   (d) With a pulse train having 1V amplitude 50μs period and 20μs pulse duration as an input, plot the corresponding output voltage. Define and measure the rise time of the output of your amplifier. Does fall time equal rise time?

   (e) Satisfy yourself that the gain of the amplifier circuit is dependent on the ratio of the resistances only.

3. For the amplifier with a gain of $+10$,

   (a) Apply a sinusoidal voltage waveform of suitable amplitude to the input of the amplifier (you may need to use a voltage divider to reduce the signal generator voltage), and verify their gain.

   (b) Use the same input signals as in step 2(c and d), record the output voltage limits, and rise and fall times of the amplifier circuit. Compare results with those obtained for the inverting amplifier circuit in step 2.

4. For the inverter (circuit with gain -1) and follower (circuit with gain $+1$)
   (a) Apply a sinusoidal voltage waveform of suitable amplitude to the input of the amplifier and verify their gain.
   (b) Record and explain the effect on the output when the compensating resistor R_x is set to zero and 10 times R_f. For what experimental value of R_x does the DC offset become zero?
5. Verify the designs of preliminary question 3.
   (a) Let V_x be a sine wave and V_y a square wave of same frequency. Plot one cycle of V_x, V_y, and V_o for each circuit.
   (b) From the data in part (a), verify the operation of the circuits.

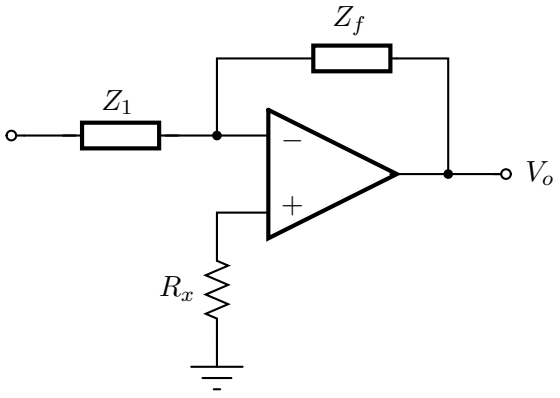

Figure 3:

Report

In your report include your analysis of the circuits and a comparison of your expected and your actual results.

Purpose

To investigate the effect that feedback has on the overall operation of the amplifier and how various mathematical operations may be realized by means of specific types of feedback.

Parts

- 1 - 741 Operational Amplifier
- Assorted resistors and capacitors

Theory

An operational amplifier (op-amp) is an analog circuit element that can perform many mathematical operations on the analog input signals. Some of these operations are additions of two signals, multiplication of a signal by a constant, integration of a signal, and differentiation of a signal.

Most of these operational circuits can be understood and analyzed using a simple ideal op-amp model for the "real" op-amp. The following are the characteristics of the ideal op-amp as shown in Figure 1(a):

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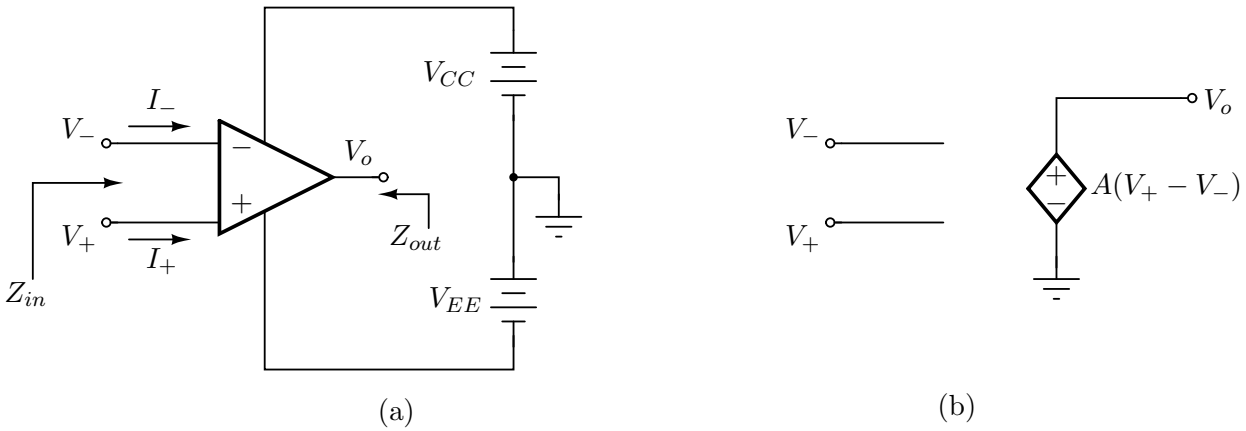

(a) (b)

Figure 1:

741 OpAmp Terminals

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4. Negative Power Supply Connection $V_{PS-} = -15$ V.
5. NC
6. Output V_o
7. Positive Power Supply Connection $V_{PS+} = +15$ V.
8. NC

Preliminary Questions

1. For the circuit of Figure 2, obtain an expression for the instantaneous value of v_o as a function of v_i if
   (a) Z_f is a capacitor and Z_1 is a resistor.
   (b) Z_f is a resistor and Z_1 is capacitor.
2. Design an integrator with $C = 1\mu$F for which $v_o = -(10^3 \text{sec}^{-1}) \int v_i dt$
3. Design a differentiator with $C = 1\mu$F for which $v_o = -(10^{-3}\text{sec})\frac{dv_i}{dt}$.
4. Plot v_o for questions 2 and 3 if v_i is a square wave that changes between ± 2.5V and has a period of 1 ms. If the square wave is perfect (no time required for transition between voltage values) and the op amp is ideal, the differentiator would produce an infinite voltage. Since perfect square waves and ideal op amps are not available in practice, the infinite voltage is not obtained. For this problem, assume that the square wave has a trapezoidal shape with a transition time of 50μs and that the op amp is ideal.

Procedure

1. As you construct the circuits from the preliminary questions **be sure to keep the Power Supply turned OFF until you are sure a particular circuit is constructed correctly**.
2. For the design of the preliminary question 2:
   (a) Describe and explain the behavior of the integrator circuit for a square wave input with an input frequency less than and greater than the period of the signal to be integrated (i.e. RC).

(b) Due to the non-ideal characteristics of an op amp i.e. input offset voltage and input bias currents the output of the integrator will drift when no input signal is applied. To investigate drift, connect the input of the integrator to ground and discharge the capacitor. Monitor the output of the integrator with a scope set to a very low time base. Repeat this drift experiment with different settings of the offset potentiometer.

(c) Use a large resistor R_p in parallel with the capacitor to eliminate dc voltage drift at the output. Verify your design with a 10 kHz square wave input. Lower resistor R_p until the output deviates from the expected result. Record R_p and explain the effect of R_p to the circuit. **NOTE: Do not dismantle this circuit, as it is required in part 4.**

3. Verify the design of preliminary question 3 using 10 kHz square wave signal. The differentiator circuit is prone to high frequency oscillation. If this should occur, use a small capacitor in parallel with the resistor. **Determine the effect of changing C and R-values.**

4. Apply the output of the integrator circuit to the input of the differentiator circuit and see if the original square wave may be reconstructed.

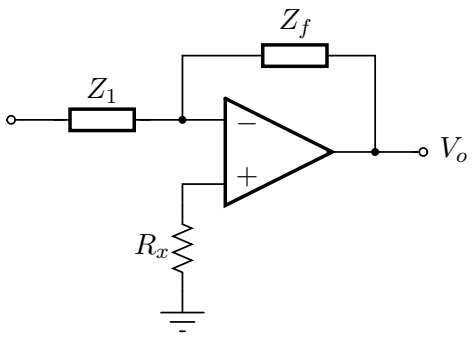


Figure 2:

Report

In your report include your analysis of the circuits and a comparison of your expected and actual results. Include sketches of the input and out voltages as observed on the scope.

Introduction

Be sure to print a copy of Experiment #4 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring graph paper (cm × cm is best).

Here are some additional comments regarding this experiment:

1. Your kit may have a 1N4006 not a 1N4004 standard diode. Note that the 1N4735 is a Zener diode.
2. The voltage on Channel 1 (X) in Figure 4 will be $-v_D$ not v_D. You will need to change the polarity on the scope to display ($-X$) so that positive values of v_D scan to the correctly on the display.
3. **WARNING**: Do not accidentally apply a high voltage (> 0.8 V) directly across the diode as v_D. Why?

Preliminary Preparation

There is a not a great deal of preparation required for this experiment. Your data will be graphical. Some of the plots are i vs. v and some are i (or v) vs. time. So, have some graph paper. You may not want to put on the scales until you see what is on the scope.

Purpose

In this experiment, you will examine the v-i characteristics of the pn-junction diode and consider its use in some simple circuits.

Parts

- 1 - 1N4004 (or 1N4006)
- 1 - 1N4735

Theory

A pn-junction diode is fabricated of p-type and n-type semiconductor material. It is a two-terminal device. The terminal connected to the p-type material is called the anode; the terminal connected to the n-type material is called the cathode.

A diode is an inherently non-linear device that conducts current when the voltage across it is of one polarity and does not conduct current when the voltage across it is of the other polarity. Using the notation shown in Figure 1 we can write

$$\begin{aligned} v_D > 0 \quad &\rightarrow i_D = \text{large and positive} \\ v_D < 0 \quad &\rightarrow i_D = \text{small and negative} \end{aligned}$$

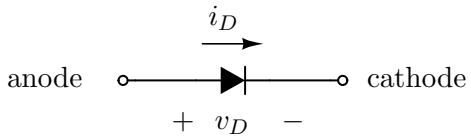


Figure 1:

An analytical expression relating i_D and v_D is given as follows and is graphed in Figure 2.

$$i_D = I_s \left[\exp\left(\frac{v_D}{nV_T} \right) - 1 \right]$$

where $V_T = kT/q$ and is called the thermal voltage ($\approx$ 26mV at room temperature), n is a grading factor (ranging from 1–2) and I_s is the saturation or scale current (usually in the pA range).

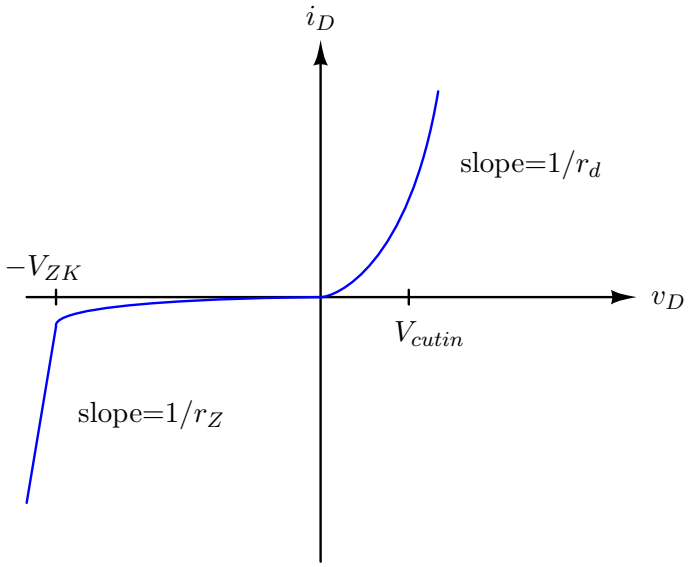


Figure 2:

The expression given above is valid only for steady-state conditions. When the diode voltage is switched suddenly from one value to another the current can be considerably different from that indicated above. Switching from no bias or reverse bias to forward bias is a relatively fast process in a pn-junction diode, and the current given by the ideal diode equation above is quickly established. The same can not be said about the opposite switching procedure, however. When a diode is forward biased in has a large amount of excess charge in the region near the pn-junction. When the diode is reverse biased or unbiased it does not. Thus when the diode is switched from forward to reverse bias a large reverse current flows until this charge is removed. The time it takes for this to occur is called the storage time, or t_s. After the storage time the current gradually reverts to its steady-state value. The total time after it takes for the diode current and voltage to go to their steady-state values is referred to as the reverse recovery time, or t_{rr}. See Figure 6 for the practical laboratory definitions of t_s and t_{rr}. Note that the term *bias* means applied voltage.

Procedure

1. *i-v* **Curve - Point-by-point method**
   Set up the circuit shown in Figure 3 using a 1N4004 (or 1N4006). You will want to measure the exact value of R_x using the ohmmeter function of your DMM. Use the following values for V_{BB}: -2 V to -20 V in increments of -2 V, and 0.1 V to 2 V in units of 0.1 V. For these values measure i_D and v_D using the DMM. The easiest way to find i_D is to measure v_x and calculate i_D using Ohm's Law. Note that it may be necessary to use different values of R_x to get the desired range of currents. Make sure to choose values of R_x which will allow you to plot the *knee* in the *i-v* characteristics at $v_D = V_{cutin}$. The cut-in voltage V_{cutin} is the voltage at which the diode current i_D changes abruptly. You will not be able to measure the reverse breakdown characteristics of this diode since it occurs at such large negative voltages. Record the i_D-v_D data, plot i_D vs. v_D. In your report, compare your data with the theory.

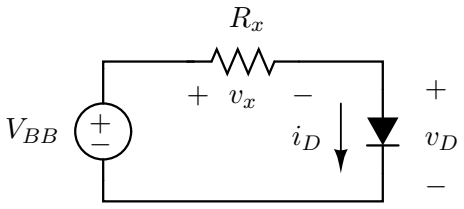


Figure 3:

2. *i-v* **Curve - Oscilloscope Display**
   Connect the circuit shown in Figure 4. You are going to use the oscilloscope in the *X-Y* mode, which is different from the usual time-base sweep mode. We will also use the storage feature on the digital oscilloscope. Here, we want to measure v_D along the x-axis (Channel 1) and i_D (or equivalently v_y) along the y-axis (Channel 2).

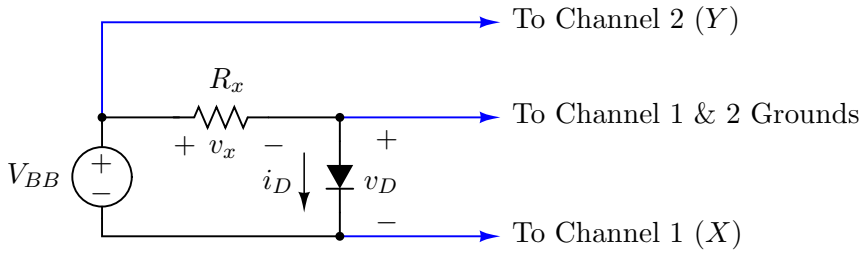


Figure 4: Note that Channel 1 (X) will show $-v_D$ instead of v_D.

Here's the setup for the scope:

(a) Press Main/Delayed (hard key)

(b) Choose XY mode (soft key)

(c) Invert x-axis using button 1 (hard key then soft key)

Set V_{BB} to zero. Set volts/div (sensitivity) of Channel 1 to 200mV/div. Set volts/div of Channel 2 such that each division on the vertical axis represents 1.0 mA. Adjust the position knobs so the "dot" on the scope screen is centered. Push the AUTO-STORE button; "STORE" should be visible in the upper left of the scope screen. Increase V_{BB} and note the

forward bias characteristic of the diode. Turn off the storage feature by pushing the AUTO-STORE button. Return the "dot" to the scope screen center by setting V_{BB} to zero.

Reverse the leads on V_{BB} and repeat the procedure of the above paragraph to obtain the reverse bias characteristic. For the forward biased diode, estimate the cut-in voltage and dynamic resistance, r_d (from the slope of the i_D-v_D curve).

3. **Measurement of Zener breakdown voltage**
   Use a 1N4735 diode for this part of the experiment. Connect the circuit of Figure 4 so that you can measure the reversed biased characteristic using the technique of Section 2. Determine the breakdown voltage V_{ZK} and estimate the Zener resistance r_Z.

4. **Measure of the Storage Time and Reverse Recovery Time**
   Setup the circuit of Figure 3, except with the DC power supply replaced by the pulse generator. Use the 1N4004 (or 1N4006) diode. Set up the pulse generator to produce the waveform shown in Figure 5. Display the diode voltage and current on the oscilloscope. How do they compare with the expected waveforms indicated in Figure 6? Determine the storage time t_s and reverse recovery time t_{RR} of the diode.

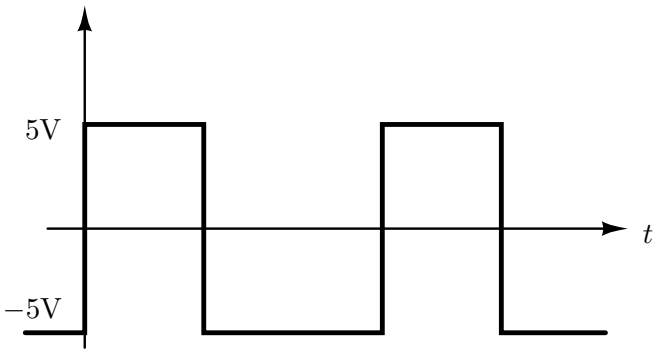


Figure 5:

Report

In your report include your sketches of the waveforms from the scope. And include any comparison between the expected and actual results.

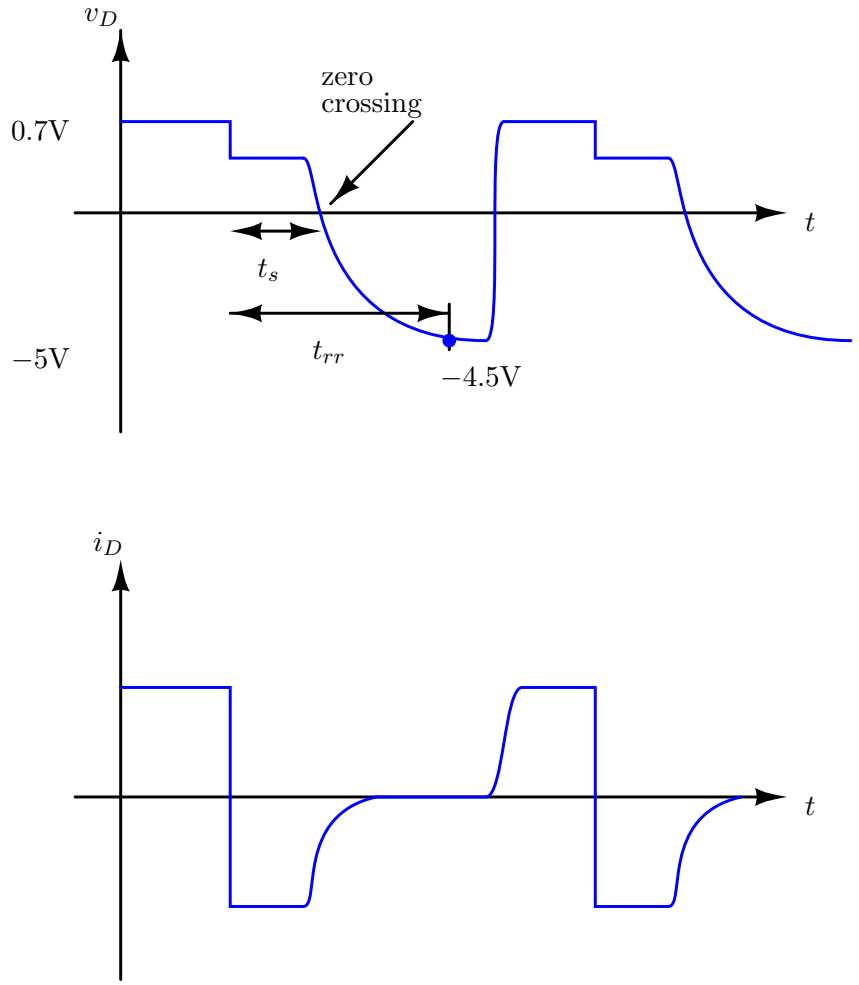


Figure 6: The plots are not to scale. The value of -4.5V is 90% of the final value (-5V) of the waveform.

Introduction

Be sure to print a copy of Experiment #5 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring graph paper (cm × cm is best).

Preliminary Report Requirements

Due at the beginning of your lab session. **No late work will be accepted!** Data/graphs and circuit analysis will be graded separately. Your work must be neat. If the TAs can't read your writing then your work is wrong. Read experiment 5 very carefully. It should be obvious what needs to be prepared in advance.

You may assume that the diode on model is a battery with $V_{D,on} = 0.7\text{V}$ in series with a resistor $r_{D,on} = 0\Omega$. The off model is, of course, an open circuit.

1. Background
   (a) Review diode circuit analysis techniques
   (b) Read about Logic Gate Noise Margins (Sedra & Smith, pages 1062-1065)
2. Data Tables and Graphs (will be returned to you in lab same day of submission)
   (a) Data Tables – set up data tables for all of the measured data that you expect to record for this experiment.
   (b) Graphs – prepare graph paper with appropriate labels and units for the sketches of the images that you will be displaying on the scope.
3. Circuit Analysis (will be returned the next lab session. Better keep a copy for your report.)
   (a) For the circuit in Figure 1 let $V_r = 2.5\text{V}$ and consider four cases for voltages V_A and V_B.
   - $V_A = 0\text{V}$; $V_B = 0\text{V}$
   - $V_A = 5\text{V}$; $V_B = 0\text{V}$
   - $V_A = 0\text{V}$; $V_B = 5\text{V}$
   - $V_A = 5\text{V}$; $V_B = 5\text{V}$

   For each of the four combinations of V_A and V_B find:
   i. The voltage across each diode
   ii. The current in each diode
   iii. The output voltage V_{out}
   iv. The current in the 1kΩ resistor

   Be sure to show all of your work!
   (b) Repeat the above for the circuit in Figure 3. **Be sure to show all of your work!**
   (c) Repeat the above for the circuit in Figure 6 under these conditions
   - $V_{in} = 0\text{V}$
   - $V_{in} = 5\text{V}$

   Be sure to show all of your work!
   (d) Verify that the expression at the end of Theory part 1 is correct for the given conditions. **Be sure to show all of your work!**

(e) Noise Margins – Calculate the noise margins HIGH and LOW for the circuits in figures 1 and 3.

4. Be sure to have your data checked and signed off by your TA before you leave the lab.

Purpose

In this experiment, you will investigate the switching properties of diodes and practice characterizing logic gates.

Parts

- 3 - 1N4148 small signal diodes

Theory

In the discussion below we will model a diode current-voltage characteristics using the constant voltage drop model. In this model we assume that no current flows through the diode if it is reverse biased or has a forward bias less than some voltage $V_{D,on}$. Once the diode is forward biased to this extent it can conduct any current, but the voltage drop remains at the constant voltage $V_{D,on}$. Thus we are considering the diode to be a perfect current switch with a threshold voltage of $V_{D,on}$. This voltage is the range 0.6–0.8 V for silicon diode, and 0.3–0.5 V for germanium or Schottky barrier diodes.

1. *Voltage Transfer Characteristics (AND Gate)*
   A diode AND gate is shown in Figure 1 and the voltage transfer characteristics are sketched in Figure 2. The circuit is designed such that all of the diodes are reverse-biased (off) when both input voltages are HIGH (5V). If either one of the input voltages are decreased below $V_{DD} - V_{D,on}$ then the corresponding input diode becomes forward-biased (on) and a current starts to flow through the resistors. The output voltage will then decrease due to the voltage drop across the 10kΩ resistor. V_{out} will continue to decrease as either of the input voltages decreases until D_3 becomes forward-biased. This occurs when V_{out} decreases to $V_r - V_{D,on}$. This is as low as the output voltage can go since the voltage drop across D_3 is approximately constant as long as it is forward-biased. An analysis of the circuit at the point where D_3 just starts to conduct reveals that at least one of the input voltages must be, as low as,

$$V_{IL} = V_r - 2V_{D,on} - \left(\frac{R_1}{R_2}\right)[V_{DD} - V_r + V_{D,on}]$$

   The other input voltage must be greater or equal to this voltage.

2. *Voltage Transfer Characteristics (OR Gate)*
   A diode OR gate is shown in Figure 3. Note that $V_r = 2.5$V should be connected from the cathode of D_3 to ground. The voltage transfer characteristics are sketched in Figure 4. The circuit is designed such that all of the diodes are reverse-biased (off) when both input voltages are LOW (0V). If one of the input voltages is increased above $V_{D,on}$ then the corresponding

input diode becomes forward-biased (on) and current starts to flow through the 10kΩ resistor. The output voltage will then increase due to the voltage drop across the 10kΩ resistor. Output voltage V_{out} will continue to increase as either of the input voltages increase until D_3 becomes forward-biased. This occurs when V_{out} increases to $V_r + V_{D,on}$. This is as high as the output voltage can go since the voltage drop across D_3 is approximately constant as long as it is forward-biased. At the point where D_3 just starts to conduct one of the input voltages must be $V_r + 2V_{D,on}$. One diode forward bias voltage drop for D_3 and one for the input diode. The 1kΩ resistor is just starting to conduct and does not yet have a voltage drop due to current flow. The other input voltage must be less than or equal to this voltage.

3. *Propagation Delay*
Due to circuit capacitances, including the internal capacitances of semiconductor devices, there is a delay from the time a signal is applied to the input and the time the corresponding output voltage appears. The turn-on delay time, the time for the output voltage to go from LOW to HIGH is called t_{PLH}. The turn-off delay time, the time for the output to go from HIGH to LOW is called t_{PHL}. The average propagation delay, called t_{PD}, is the average of the turn-on and turn-off times if a 50% duty cycle is assumed,

$$t_{PD} = \frac{t_{PLH} + t_{PHL}}{2}$$

The propagation delay times are defined by the halfway points on the input and output signals as shown in Figure 5.

Procedure

1. *Truth tables*
Set up the circuit of Figure 1. Use a value of 2.5V for V_r measure the output voltage for each of the combinations of input voltages $V_A, V_B = 0, 5\text{V}$. Verify that circuit performs as an AND gate. Set up the circuit of Figure 3. Measure the output voltage for each of the combinations of input voltages. Verify that the circuit behaves as an OR gate.

2. *Voltage transfer characteristics*
Set up the circuit shown in Figure 6. Use a value of 2.5V for V_r displays the voltage transfer characteristics, V_{out} versus V_{in}, using the X–Y mode of the oscilloscope. Sketch the results. Note the voltage levels corresponding to V_{OH}, V_{OL}, V_{IL}, and V_{IH}. Using these values determine the logic swing, the transition width, and the noise margins. Why cant this gate be used in real digital applications?

3. *Propagation delay time*
Replace the power supply at the input terminals with a pulse generator and adjust the amplitude to reproduce the waveform of Figure 7. Measure the propagation delay time. Sketch the waveform. Increase the frequency of the pulse generator gradually and determine the maximum cooperating frequency of the gate.

Report

Answer the questions requested in the above procedures. Calculate the theoretical logic swing, transition width, and noise margins and compare with your measured values. Assume a value of

0.7V for $V_{D,on}$. Determine the average propagation delay using your measured values and assuming a 50% duty cycle.

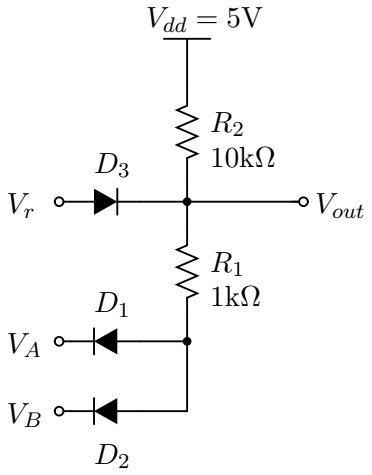


Figure 1: AND gate.

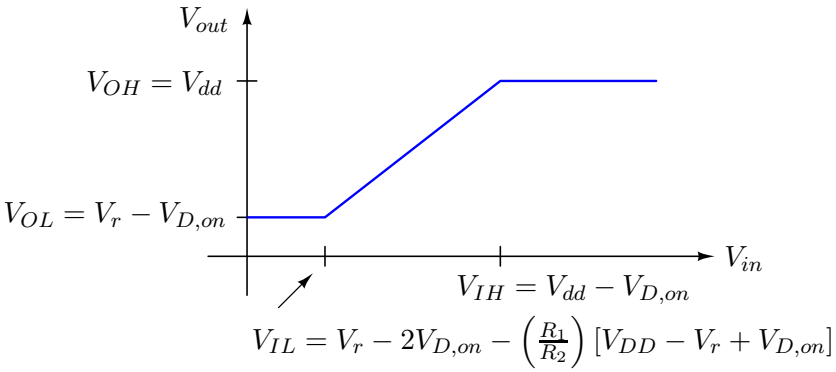


Figure 2: AND gate characteristics.

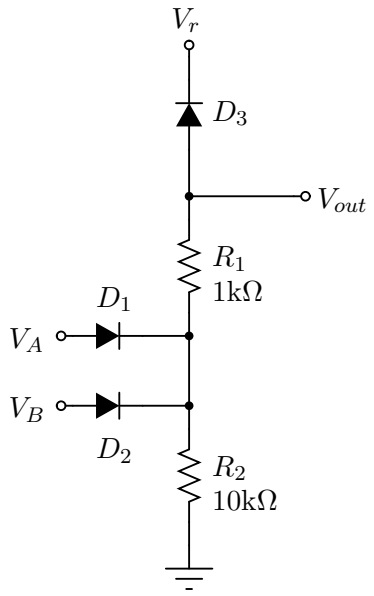


Figure 3: OR gate.

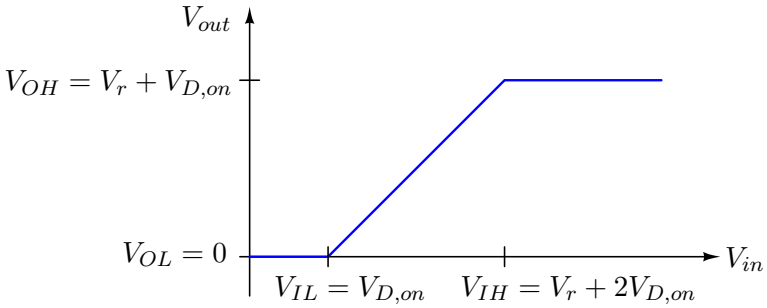


Figure 4: OR gate characteristics.

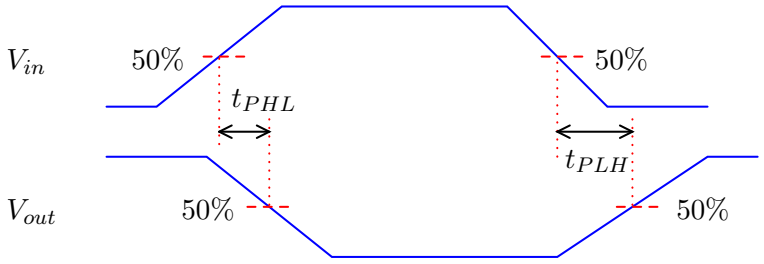


Figure 5: Propagation delay.

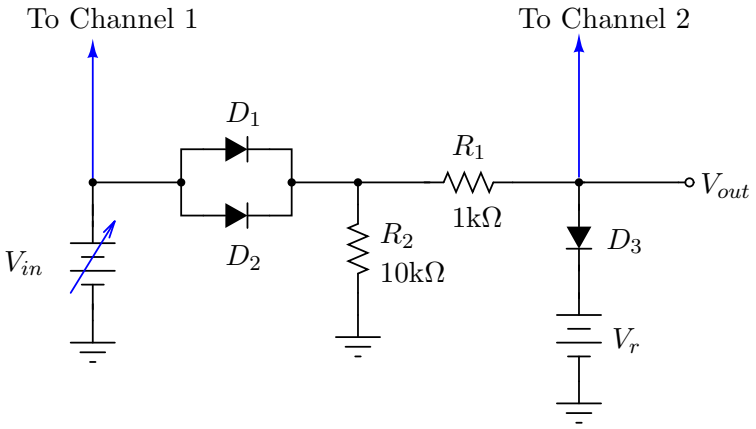


Figure 6:

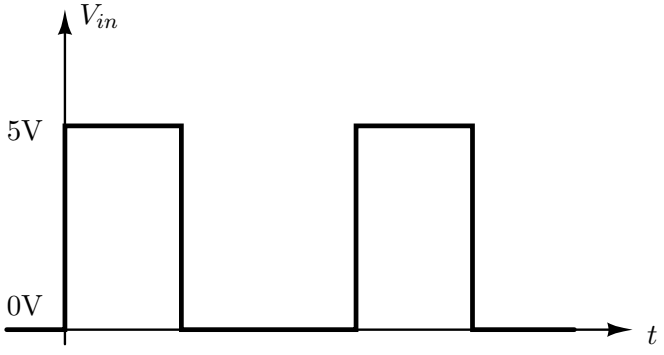


Figure 7:

Introduction

Be sure to print a copy of Experiment #6 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring graph paper (cm × cm is best).

Preliminary Report Requirements

You should do the following in preparation for the experiment.

1. Assume the following circuit values:
   (a) $V_s = 10\sin(\omega t)$, where $\omega = 120\pi$ (except circuit of Figure 2)
   (b) $C = 10\mu$F,
   (c) $R_L = 27$kΩ,
   (d) $R_x = 1$kΩ (or greater)
   (e) V_{on}(forward) = 0.6V
   (f) V_z(reverse) = −5.8V (Or, use what you found for the zener breakdown value for the zener diode in your kit.
   (g) $R_s = 50\Omega$ (Function generator internal resistance.)
2. Analyze the circuits in the Figures 1 to 5.
3. Sketch the expected graphs of $V_s(t)$, $V_g(t)$, and $V_L(t)$.
4. Find the peak value and the average DC value of the load voltage V_L.
5. For the DC Power Supply circuit in Figure 2, find the ripple voltage V_r and average DC value of V_L with
   (a) $\omega = 120\pi$ and
   (b) $\omega = 1200\pi$
6. For the Zener Regulator circuit in Figure 3, calculate the minimum value allowable for R_L and still have good voltage regulation. Diode is "just ON reverse" at the voltage V_Z.
7. Be sure to complete the above before the lab session.

Note that in every case you must first find the range of values of V_S that keep the diode(s) OFF. (i.e. What range of V_s guarantees $V_d < V_{on}$?) Then, assume that range, use the open circuit model for diode, and, do circuit analysis. Next, assume V_s takes on the remaining range of values; therefore, the diode must be ON. Replace the diode with the required ON model and do circuit analysis.

Purpose

The circuits in this experiment represent some of the most common and practical uses of diodes. Every electrical engineer should be familiar with the operation and analysis of these circuits. The fundamental concepts of these circuits are covered at length in your text and will not be reviewed here.

Parts

- 1 - 1N4004 (or 1N4006) diode
- 1 - 1N4375 zener diode
- 1 - 10μF capacitor
- assorted resistors

Procedure

Note that the data from this experiment are the sketches of the voltages that are taken right off the scope.

1. Set $V_s(t) = 10\sin(120\pi t) = 7.07$V RMS . Do this by measuring V_g without anything connected to the function generator.
2. Construct the circuits and measure (i.e. sketch) the graphs of $V_s(t)$, $V_g(t)$, and $V_L(t)$. Compare the sketches to your predictions of your preliminary work. If they are extremely different, your circuit may not be setup correctly.
3. For each circuit, use the DMM as a DC voltmeter and measure the DC value of V_L. Compare this to your calculated values.
4. For the DC Power Supply circuit in Figure 2, be sure to measure V_r and the DC value of V_L at frequencies 60Hz and 600Hz and compare the values to your preliminary calculations.
5. For the Zener Regulator circuit, try attaching smaller and smaller values of R_L until you find the minimum R_L allowable and still have good regulation. Compare to your calculated minimum value.
6. **Answer the following sets of questions for all circuits**: What happens when you remove R_L and just leave an open circuit. Does the circuit performance improve? For the doubler circuit try different values of R_x and observe the effect on V_L. What value of R_x drives V_L to a maximum value?

Report

For your written report:

1. Include preliminary calculations and sketches.
2. Include your data. i.e. the sketches of voltages from the scope.
3. Explain the discrepancies between calculated and actual experimental values. Example: Why is V_g so distorted when the circuits are attached to the function generator?
4. Any conclusions about the performance of the circuits and the questions that you have answered.

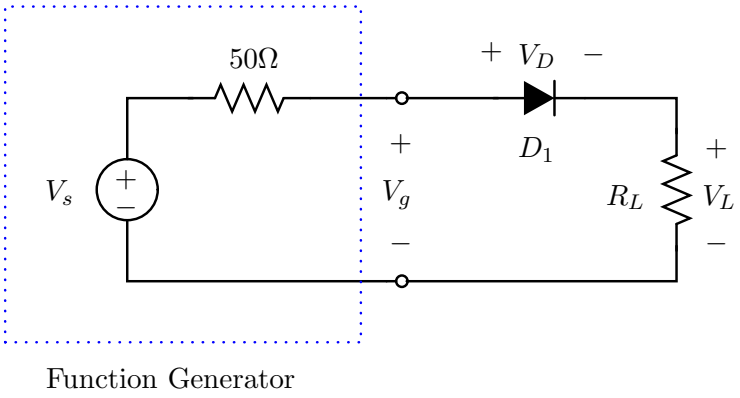


Figure 1: **Half-Wave Rectifier** This circuit clips off the negative peaks of the pure AC sine wave. The result is a voltage with a positive average value. So, we have converted AC to DC.

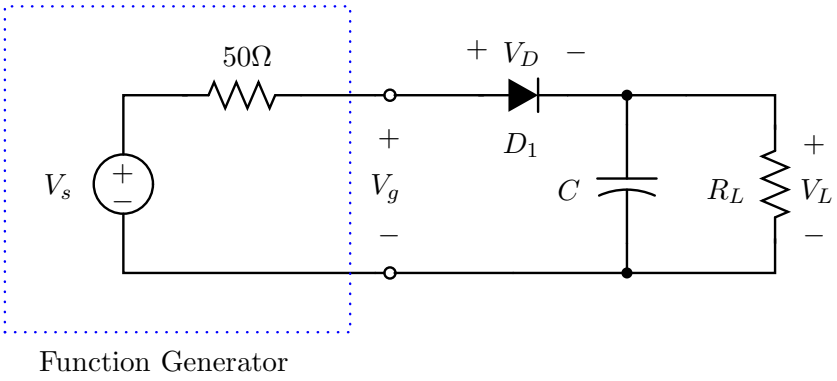


Figure 2: **The DC Power Supply** This circuit is the half-wave rectifier with a filter capacitor. The capacitor "holds up" the voltage so that the average DC value of the output voltage V_L is almost the same magnitude as the magnitude of the input AC sine wave!

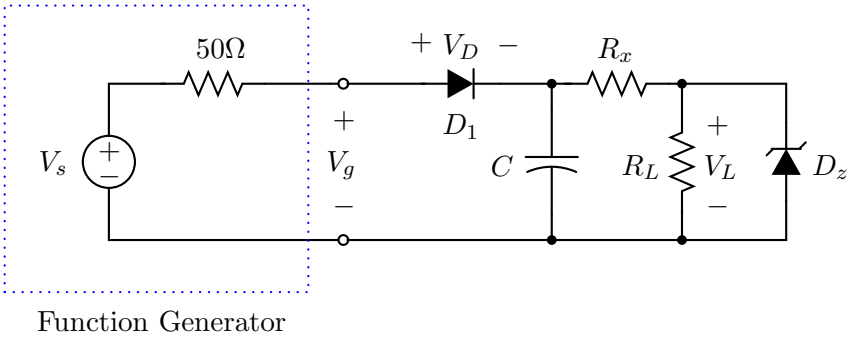


Figure 3: **The Zener Voltage Regulator** Note the addition of resistor R_x to the circuit. Without resistor R_x the output voltage cannot be pure DC which is our goal. We also require that $\frac{R_L}{R_L+R_x}(V_{g,max} - V_{d,on}) > |V_Z|$ to have pure DC output. Therefore, we need to have $R_L >> R_X$. The Zener Diode removes the ripple voltage that "rides on the DC value" of the power supply circuit above. We lose some magnitude but we gain a pure DC output as long as R_L is not too small.

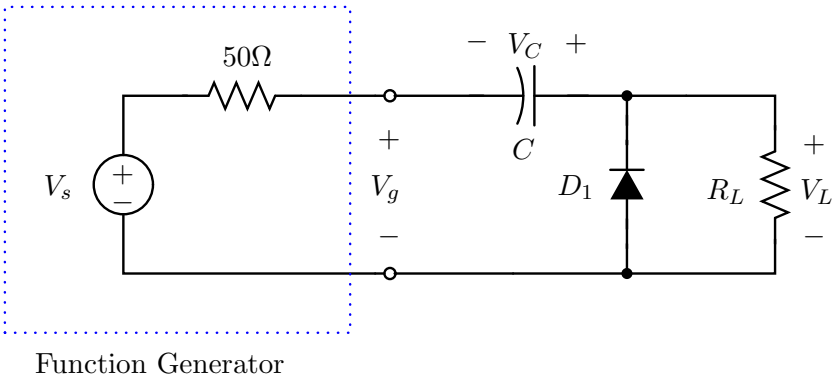


Figure 4: **The Voltage Doubler** In this circuit, we get the AC sine wave input to "ride on a DC" value equal to the magnitude of the sine wave input. The result is a "peak output voltage" that is twice the magnitude of the AC input peak. Note that the capacitor charges when the diode turns on and (if R_L is sufficiently large) does not discharge much. That's our free ride, the charge on the capacitor. This circuit is also called a "diode clamper."

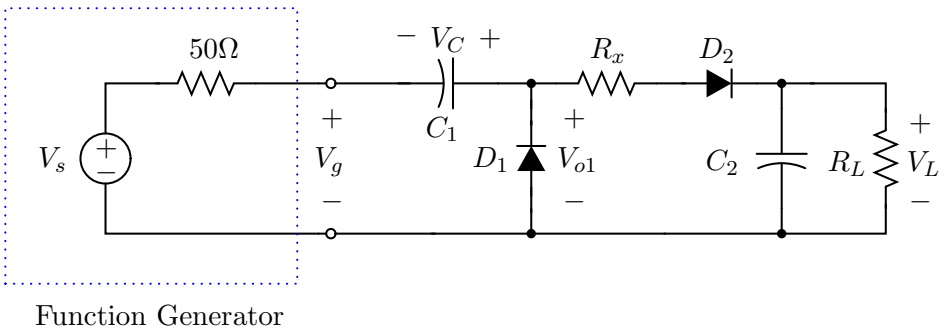


Figure 5: **Voltage Doubled DC Supply** Here we first double the input voltage with a voltage doubler circuit. Next, we connect that output to the input of a half-wave rectifier with filter capacitor. The resulting final output voltage is a DC voltage (almost) twice the value of the magnitude of the input AC sine wave! And they say you can't get something for nothing ...

Introduction

Be sure to print a copy of Experiment #7 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring graph paper (cm × cm is best).

Purpose

You will measure the *i-v* characteristics of a transistor and explore the transistor in amplifying circuits.

Parts

- 1 - TN3019A NPN transistor

Theory

The bipolar junction transistor (BJT) is a three-terminal device that can be used as a switch or an amplifier. BJTs are fabricated by sandwiching one type of semiconductor material between regions of the other type. Hence, there are two varieties of BJTs – NPN or PNP. Refer to Figure 1, note that the three terminals are the base, emitter, and collector. Although the diagrams make it appear that collector and emitter terminals may be interchanged, in real transistors this can **not** be done.

In order to use the transistor as an amplifier, the transistor must biased into the active region. In the active region (1) the emitter-base junction must be forward biased, (2) the collector-base junction must be reversed biased, and (3) the collector-emitter voltage is greater than $V_{CE,SAT}$ and less than V_{CC} (see Figure 3). In the active region, (l) the transistor base current is very small. Hence, the emitter and collector current magnitudes are about the same. (2) The collector current is independent of the collector-base voltage, (3) and the collector current is a strong function of the base-emitter voltage. Thus, small changes in the base-emitter voltage causes large changes in the collector current. This is the mechanism of amplification; a small change in one part of the circuit causes large changes in another part of the circuit.

Procedure

1. *Collector i-v Characteristics of a BJT* – Connect the circuit shown in Figure 2.

   - Scope set-up: Option Press
   - XY Operation Main/Delay
   - Inverter x-axis 1(button)

   Set $V_{BB} = V_{CC} = 0$. Use the position knobs on Channel 1 and Channel 2 to position the "dot" to the lower-left corner of the scope screen, the origin.

   Press the AUTO-STORE button so "STORE" appears in the upper-right of the scope screen. Slowly increase V_{CC} to sweep out a curve similar to AUTO-STORE button so "RUN" appears in the upper-right of the scope screen. Slowly decrease V_{CC} so that the "dot" is returned the origin.

Set V_{BB} to a non-zero value. Repeat the steps of the above paragraph. Change V_{BB} to obtain the I_B values shown below and trace out a curve for each of these.

Notice that the horizontal input to the scope is V_{CE} and the vertical input is I_C. This will give us the i-v characteristic of the transistor. Now, adjust the DC power supply to get a base current of 25μA. Sketch the resulting trace on a graph paper and label the axes properly. Repeat the experiment by adjusting the DC power supply to get base currents of 0μA, 50μA, 75μA, and 100μA. Note that the horizontal and vertical sensitivities of the scope may have to be adjusted in order to get a trace large enough to fill the scope screen. Fill in the table below with the values obtained in the experiment.

v_{CE} (V)	I_B (μA)	I_C (mA)
5	0	
5	25	
5	50	
5	75	
5	100	

2. *Transistor as a linear amplifier* – Connect the circuit shown in Figure 3. Set the peak amplitude of the function generator to 0.25V and the frequency to 1000 Hz. Observe $i_B(t)$, $v_B(t)$, $v_E(t)$ and $v_C(t)$ on the scope and record them. Both input switches of the scopes should be set to DC. Indicate clearly the DC level and the peak-to-peak variation (swing) of the ac component of each signal on your sketch. If you observe any distortion in the $v_C(t)$ waveform, reduce the amplitude of v_i until there is no distortion. Note that if we assume linear operation with no distortion, each signal will consist of both a dc and an ac component,

$$i_B(t) = I_{BQ} + i_b(t)$$
$$i_C(t) = I_{CQ} + i_c(t)$$
$$v_C(t) = V_{CQ} + v_c(t)$$

Note also that we cannot observe the base current $i_B(t)$ and the collector current $i_C(t)$ directly on the scope.

Report

Answer the questions and draw the graphs requested in the procedures above. Is there any voltage gain in the circuit of figure 3?

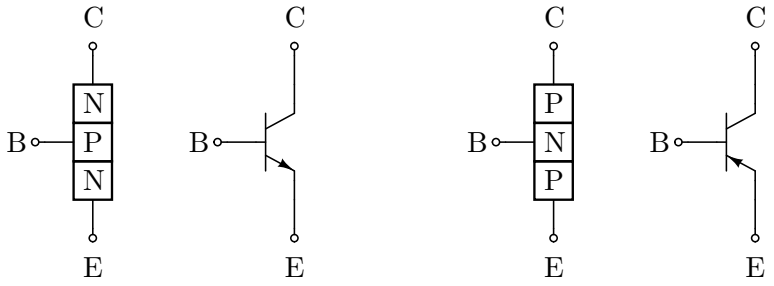


Figure 1: **Bipolar Junction Transistors** The three terminals are the collector (C), base (B) and the emitter (E). The NPN transistor, the base is p-type and the arrow at the emitter points away from the base. In the PNP transistor, the base is n-type and the arrow at the emitter points to the base.

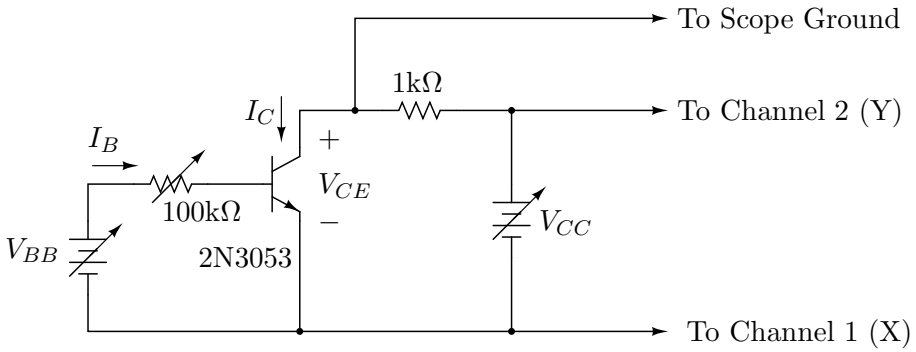


Figure 2: Circuit used to determine bipolar junction transistor characteristics.

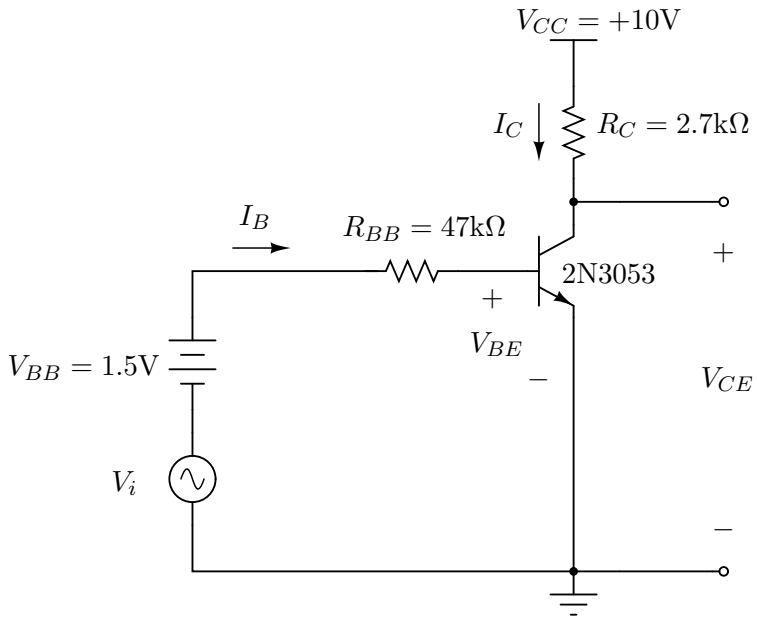


Figure 3: Simple amplifier.

Introduction

Be sure to print a copy of Experiment #8 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring graph paper (cm × cm is best).

Purpose

In this experiment, you will measure some of the important parameters of a bipolar transistor, and to study a general large-signal model, the Ebers-Moll model, that we can then simplify to obtain working models for switching circuits.

Parts

- 1 - TN3019A NPN transistor
- 2 - 1N270 Germanium diode

Theory

1. **The Ebers-Moll (EM) Model of a Bipolar Transistor** The basis for the models that we use in studying transistor circuits is referred to as the Ebers-Moll model and is shown in Figure 1. It contains two diodes (D_E and D_C) and two controlled current sources whose "contract" is to deliver currents that are proportional to the currents flowing in the diagonally located diodes. These current sources represent the effects of transistor action. Without them the model would simply reduce to two back-to-back diodes. The diodes in the model are idealized p-n junction diodes, and therefore the diode currents are given by:

$$I_{DE} = I_{SE}\left(e^{V_{BE}/V_T} - 1\right) \tag{1}$$

$$I_{DC} = I_{SC}\left(e^{V_{BC}/V_T} - 1\right) \tag{2}$$

The values I_{SE} and I_{SC} are saturation current values that are constant at a given temperature. The reference directions of voltages V_{BE} and V_{BC} are chosen so that when they are positive the diodes are forward-biased. A relationship exists between the four parameters of the EM model and the transistor scale current I_S

$$\alpha_F I_{SE} = \alpha_R I_{SC} = I_S \tag{3}$$

The currents flowing at the emitter and collector terminals can be written directly from the model in Figure 1 as follows:

$$I_E = I_{DE} - \alpha_R I_{DC} \tag{4}$$

$$I_C = -I_{DC} + \alpha_F I_{DE} \tag{5}$$

where I_{DE} and I_{DC} are the diode currents defined in (1) and (2). By combining expressions in (1)–(5), the terminal currents can also be expressed in terms of the applied voltages V_{BE} and V_{BC} as

$$I_E = \frac{I_S}{\alpha_F}\left(e^{V_{BE}/V_T} - 1\right) - I_S\left(e^{V_{BC}/V_T} - 1\right) \tag{6}$$

$$I_C = I_S\left(e^{V_{BE}/V_T} - 1\right) - \frac{I_S}{\alpha_R}\left(e^{V_{BC}/V_T} - 1\right) \tag{7}$$

The base current can be determined from Kirchhoff's current law and is found to be

$$I_B = I_E - I_C \tag{8}$$

Hence, using (4) and (5),

$$I_B = I_{DE}\left(1 - \alpha_F\right) + I_{DC}\left(1 - \alpha_R\right) \tag{9}$$

or using Eqs. (6) and (7),

$$I_B = \frac{I_S}{\beta_F}\left(e^{V_{BE}/V_T} - 1\right) + \frac{I_S}{\beta_R}\left(e^{V_{BC}/V_T} - 1\right) \tag{10}$$

where

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \tag{11}$$

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R} \tag{12}$$

Equations (6) and (7) describe what is called the Ebers-Moll (EM) model of the transistor. This mathematical model provides very useful general relationship that applies to a transistor under any bias condition. However, as was true for diodes, we find that some key approximations can greatly simplify the model while keeping it accurate enough for many applications. Our modified models will permit us to do this.

2. **Normal-mode Active-region Models** We define the normal-mode active region for the following conditions:

   (a) Base-Emitter Voltage V_{BE} is equal to or larger than the threshold voltage of diode D_E.

   (b) Base-Collector Voltage V_{BC} is less than the threshold voltage of diode D_C.

   In this latter case I_{DC} can be treated as zero. Hence in Figure 1 the diode D_C and the current source $\alpha_R I_{DC}$ can be dropped out of the model to give us the model shown in Figure 2. Under these conditions the expression for I_C becomes

$$I_C = \alpha_F I_E = \alpha_F \frac{I_B}{1 - \alpha_F} \tag{13}$$

   Hence, from (11)

$$I_C = \beta_F I_B \tag{14}$$

The term β_F is called the forward (as opposed to reverse) dc current gain of a transistor and is a parameter most commonly given on discrete-transistor data sheets. On transistor data sheets, this parameter is sometimes called h_{FE}. Nevertheless, common practice is to refer to this as beta (β).

In digital ICs, β_F is centered around approximately 60, while for the linear ICs it is approximately 200. If necessary, the value of α_F can be determined from by β_F by transposing (11) to obtain

$$\alpha_F = \frac{\beta_F}{\beta_F + 1} \tag{15}$$

3. **Inverted-mode Active-region Model** In certain applications of transistors we will find that the collector is forward-biased and the emitter is reverse-biased. This condition is referred to as inverted operation. The operating conditions are then

   (a) V_{BC} is equal to or larger than $V_{BC,on}$.

   (b) V_{BE} is less than $V_{BE,on}$.

   Hence, I_{DE} is treated as zero, and we have the model given in Figure 2. In a completely analogous fashion as in the normal-mode active-region model, we express as $-I_E$ as

$$I_E = I_1 = \frac{\alpha_R}{1 - \alpha_R} I_B = \beta_R I_B \tag{16}$$

   For digital ICs, β_R is usually less than 1 and can be as low as 0.01. For discrete transistors β_R can range from 1 to 10. We shall find in later experiments that a low value of β_R is desirable for the input transistors in a popular family of digital ICs.

4. **The Saturation Mode** Consider first the normal saturation mode. In the circuit of Figure 3(a) if a current I_B is pushed into the base and if its value is sufficient to drive the transistor into saturation, the collector current I_C will be smaller than $\beta_F I_B$. The parameter σ defined as follows

$$\sigma = \frac{I_C}{\beta_F I_B} \tag{17}$$

   serves as a measure of the extent to which the transistor has been driven into saturation. As long as $\sigma = 1$ (that is, $I_C = \beta_F I_B$), the transistor is in its active region. As σ decreases below unity, the transistor is driven progressively further into saturation.

   In saturation both junctions are forward-biased. Thus V_{BE} and V_{BC} are both positive, and their values are much greater than V_T. Thus in (7) and (10), we can assume that $e^{V_{BE}/V_T} \gg 1$ and $e^{V_{BE}/V_T} \gg 1$. Making these approximations and substituting $I_C = \sigma\beta_F I_B$ results in two equations that can be solved to obtain V_{BE} and V_{BC}. The saturation voltage $V_{CE,sat}$ can be then obtained as the difference between these two voltage drops:

$$V_{CE,sat} = V_t \ln \frac{\frac{\sigma\beta_F}{\beta_R} + \frac{1+\beta_R}{\beta_R}}{1 - \sigma} \tag{18}$$

The transistor in the circuit of Figure 2(a) will saturate (that is, operate in the reverse saturation mode) when the emitter-base junction becomes forward-biased. In this case $I_1 < \beta_R I_B$.

Procedure

1. Construct the circuit of Figure 4 and determine the parameters $\beta_F = I_C/I_B$ and $V_{BE,on}$ as a function of collector current I_C. Use I_C values of 0.5, 1, 2, 5, 10, and 20 mA. Adjust R and V_{BB} to set the I_C values. Fill in the table below with the values obtained in the experiment.

R (Ω)	V_{BB} (V)	I_C (mA)	I_B (μA)	β_F	$V_{BE,on}$ (V)
		0.5			
		1			
		2			
		5			
		10			
		20			

2. Reverse the emitter and collector leads of the transistor to determine $\beta_R = I_1/I_B$ for $I_1 =$ 0.1, 1, and 10 mA.

R (Ω)	V_{BB} (V)	I_1 (mA)	I_B (mA)	β_R
		0.1		
		1		
		10		

3. Measure $V_{BE,sat}$ and $V_{CE,sat}$ as a function of $\sigma = I_C/(\beta_F I_B)$ in the circuit of Figure 5. Record these in the table below. Also, calculate $V_{CE,sat}$ using (18) by choosing typical values from the data from Part 1 and 2 for β_F and β_R. Make a graph of $V_{CE,sat}$ vs. σ. Compare the graph computed with (18) to the actual experimental curve. Do the measured and calculated values agree? If not, explain why?

I_C (mA)	σ	I_B (mA)	$V_{CE,sat}$ (V) (measured)	$V_{CE,sat}$ (V) (calculated)	$V_{BE,sat}$ (V) (measured)
5	0.8				
5	0.6				
5	0.4				
5	0.2				
5	0.01				

Report

In your report state the results of Parts 1 and 2 above. Do the comparison requested in Part 3. Also, try to make estimates for the parameters in the Ebers-Moll model of Figure 1.

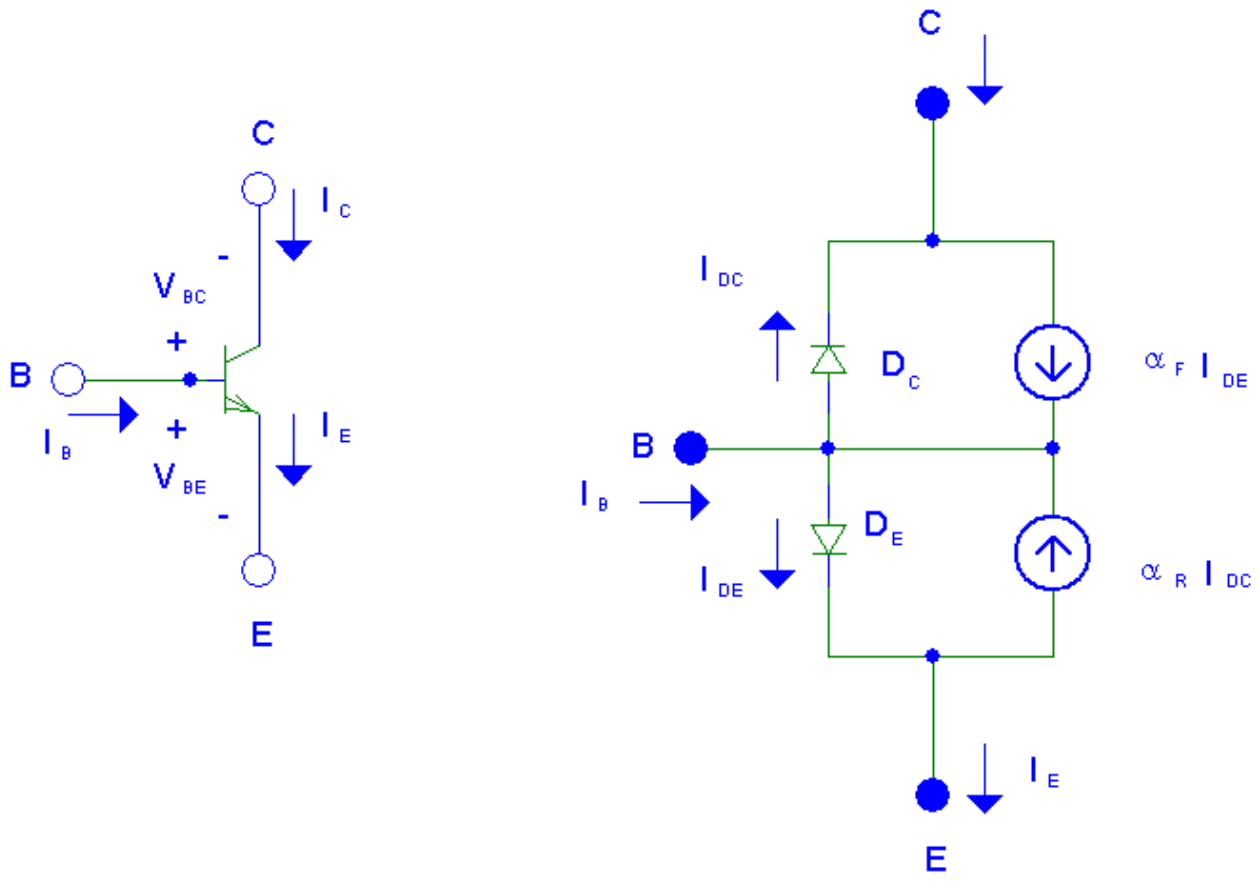


Figure 1

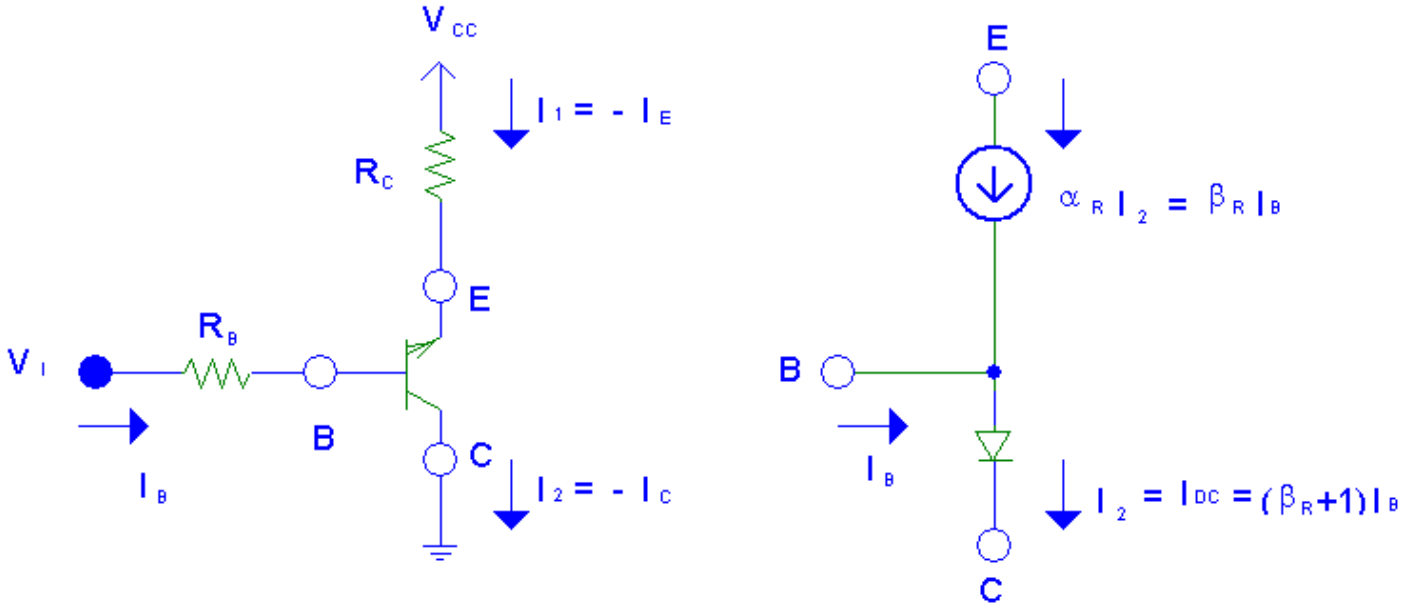


Figure 2

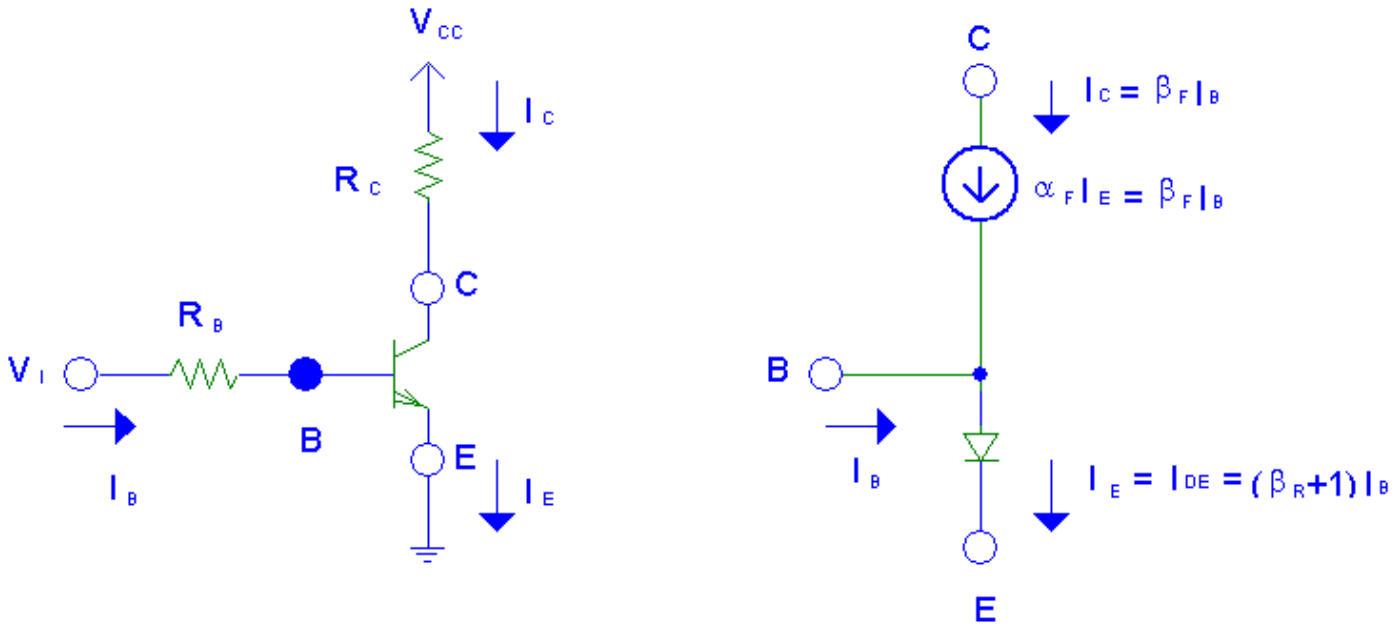


Figure 3

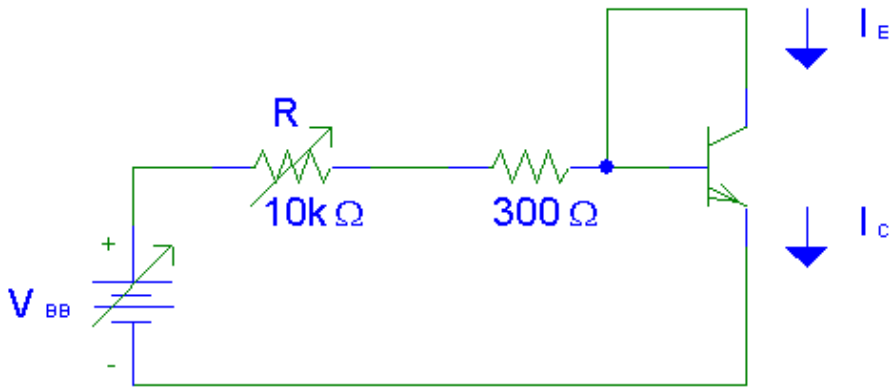


Figure 4

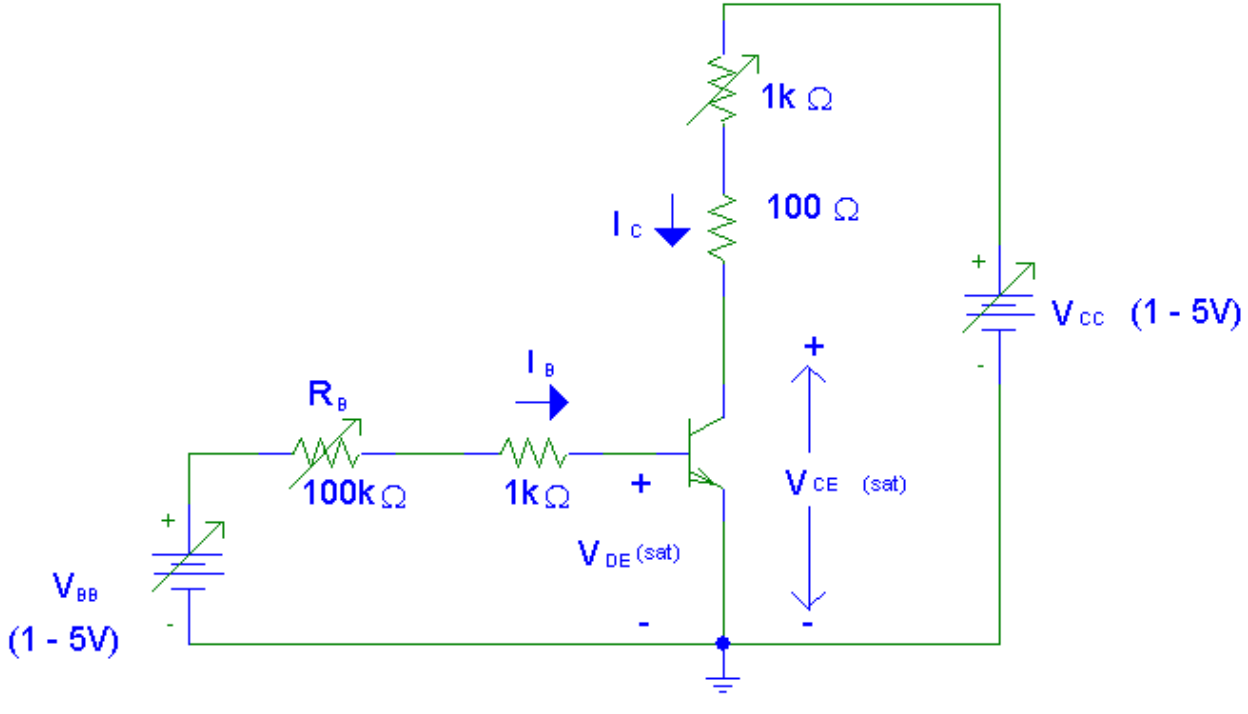


Figure 5

Introduction

Be sure to print a copy of Experiment #9 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring graph paper (cm × cm is best).

Purpose

In this experiment, you will investigate the switching properties of the resistor-transistor logic inverter.

Parts

- 2 - 2N3053 (or similar) NPN transistor
- 1 - 1N270 Germanium diode

Theory

1. **Transistor Inverter**

   A basic Resistor-Transistor Logic (RTL) inverter circuit is shown in Figure 1. For the analytical determination of the voltage transfer characteristics, we will assume the forward current gain of the transistor (β_F=I_C/I_B) is 140. The transistor will start conducting if its base-emitter voltage exceeds $V_{BE,cutoff}$=0.65V; therefore, applying input voltages below this value will result in the transistor operating in the cutoff region where all currents are zero. In the forward active region, the base-emitter voltage $V_{BE,on}$=0.7V. When the input voltage is increased further, the transistor will eventually leave the forward active region and will enter the saturation region. In saturation, the base-emitter voltage $V_{BE,sat}$=0.75V and collector-emitter voltage $V_{CE,sat}$=0.2V.

   Now let us determine the voltage transfer characteristics of the inverter shown in Figure 1. With input voltage $V_{in} < V_{BE,cutoff}$ ($V_{in} < 0.65$V), the base-emitter diode is cutoff, therefore the transistor is cutoff (I_C=0A and V_{out}=5V). When V_{in} is increased beyond 0.65V, however, base current begins to flow and the transistor moves from the cutoff region to the active region. Hence, the coordinates (V_{in}=0.65V, V_{out}=5V) mark the first breakpoint for the transfer function of this circuit. In the active region, the output voltage (V_{out}) and collector current ($I_C = \beta_F I_B$) decreases linearly with increasing the voltage input (V_{in}). This is because in the active region, the output voltage is given by

$$V_{out} = V_{cc} - R_C I_C = V_{cc} - R_C \beta_F I_B = V_{cc} - R_C \beta_F \frac{V_{in} - V_{BE,on}}{R_B} \tag{1}$$

   As V_{in} is increased further, a second breakpoint will be reached. When $V_{out} = V_{CE,sat}$, it is possible to calculate the values of I_C and I_B for this condition as follows (the subscript EOS means edge of saturation – transition between active/saturation):

$$I_{C,EOS} = \frac{V_{CC} - V_{CE,sat}}{R_C} = \frac{5\text{V} - 0.2\text{V}}{470\Omega} = 10.2\text{mA} \tag{2}$$

$$I_{B,EOS} = \frac{I_{C,EOS}}{\beta_F} = \frac{10.2\text{mA}}{140} = 72.9\mu\text{A} \tag{3}$$

Now, using the value of $I_{B,EOS}$ in the circuit of Figure 1, we find

$$V_{in,EOS} = V_{BE,sat} + I_{B,EOS}R_B = 0.75\text{V} + (72.9\mu\text{A})\,(8.2\text{k}\Omega) = 1.35\text{V} \tag{4}$$

Hence the transistor is cutoff when $V_{in} \leq 0.65$V and saturated when $V_{in} \geq 1.35$V. It operates in the active region for $0.65\text{V} < V_{in} < 1.35\text{V}$.

The breakpoints of the voltage transfer characteristic indicate where the transistor-operating region changes from cutoff to active and from active to saturation. When we use the transistor inverter as a logic gate, we have to insure that the input/output threshold levels will represent LOW and HIGH levels without any ambiguity. At the input, the threshold voltage for the LOW level is called V_{IL}; for the HIGH level, it is called V_{IH}. For the output voltage, the voltage levels V_{OL} and V_{OH} represent the low and high threshold voltages, respectively. These voltage levels are shown graphically in Figure 2.

The actual logic voltage threshold levels are set away from the breakpoints values shown in Figure 1. We choose V_{IL}=0.60V (which is *less* than the breakpoint value of 0.65V) so that an input less than or equal to V_{IL} will not turn on the transistor. We also choose V_{IH}=1.40V (which is *greater* than the breakpoint value of 1.35V) so that an input greater than or equal to V_{IH} will always saturate (turn-on) the transistor. Input levels between 0.6V to 1.4V are to be avoided because they lead to output voltage levels that are ambiguous. The difference between the two output voltages $(V_{OH} - V_{OL})$ determines the logic swing of the circuit. That is,

$$\text{Logic Swing} = V_{OH} - V_{OL} \tag{5}$$

2. **Noise Margins** Notice in Figure 2 that the output levels are compatible with the input levels in that V_{OL} and V_{OH} are located safely within the acceptable input LOW and input HIGH regions, respectively. The input LOW threshold voltage V_{IL} is 0.6V, but the output low-level voltage V_{OL} is 0.2V. Hence there is a safety margin of $V_{IL} - V_{OL} = 0.4$V. This difference determines the low-level noise margin (NML) for the circuit. That is,

$$\text{NML} = V_{IL} - V_{OL} \tag{6}$$

Similarly, the difference $V_{OH} - V_{IH}$ is the high-level noise margin (NMH). Thus,

$$\text{NMH} = V_{OH} - V_{IH} \tag{7}$$

we note from Figure 2 that an increased noise-margin capability is obtained as either V_{OH} and V_{OL} move away from each other, or as V_{IH} and V_{IL} move toward each other. Thus, with a larger logic swing or a narrower transition width, the noise margins will improve. The transition width is defined by the equation

$$\text{Transition Width} = V_{IH} - V_{IL} \tag{8}$$

3. **Fan-out** One transistor-inverter stage is generally not operated in isolation by itself; rather connection will be made from the output of one inverter to the input of one or more similar circuits. This is shown in Figure 3, where Q_0 is the driving gate and Q_1 through Q_N are the driven or load-gates. There is an upper limit to N, the number of load gates that can be connected to such as inverter output, and this is known as the fan-out of the inverter. The term fan-out is also commonly used for the number of load gates – not necessarily the limiting number.

To compute the fan-out N for the circuit shown in Figure 3, it should be noted that with a HIGH level at V_{in}, transistor Q_0 is saturated and the V_{out} will be at a LOW level. With a $V_{CE,sat}$ of 0.2V for Q_0, all the load gates will be OFF. Now consider a LOW level at V_{in}. Transistor Q_0 will be OFF with a resulting HIGH level at V_{out}. In this case it is required that the V_{out} be sufficient to ensure all the load gates Q_1 through Q_N are saturated. Each load gate added to the output of the first inverter at the collector of Q_0 will require a certain base current to cause saturation of the load transistor. The entire base current for the load gates flows through the collector resistor R_C from the 5V supply to the inputs of the load gates. An increase in the number of load gates, and consequent increase in total base current, therefore lowers the voltage V_{out}. A limit in the fan-out is set when V_{out} is insufficient to cause the transistor of the load gate to saturate. Recall from Figure 2 that this voltage is V_{IH} and is equal to 1.40V.

A simplified equivalent circuit for finding the output high voltage V_{OH} assuming a fan-out of N is shown in Figure 4. This equivalent circuit is obtained by replacing the N load transistors by a resistance RB/N in series with an ideal diode having a voltage drop equal to $V_{BE,sat}$=0.75V. From this equivalent circuit (using KVL involving V_{CC}, R_C, RB/N and $V_{BE,sat}$), we obtain

$$V_{OH} = V_{CC} - R_C \frac{V_{CC} - V_{BE,sat}}{R_C + R_B/N} \tag{9}$$

It can easily be seen that as N is increased, V_{OH} decreases. With no loading gates V_{OH} is simply V_{cc} as shown in Figure 2. However, when gates are added to the output of the first inverter, V_{OH} will decrease as shown in (9). As a result, the high-level noise margin (NMH) and the logic swing will also decrease.

4. **Power Dissipation** The power dissipation in a logic gate with all inputs at a HIGH level is called P_{DH}. With the inputs at a LOW level, the power dissipation is called P_{DL}. The average power dissipation $P_{D,av}$ is given by

$$P_{D,av} = \frac{P_{DH} + P_{DL}}{2} \tag{10}$$

This number is obtained by assuming the input to the gate spends, as much time at the LOW level as it does at the HIGH level, that is, there is a 50% duty cycle.

5. **Propagation Delay** Due to circuit capacitances and the finite switching of the transistors used, there is a delay from the time a signal is applied to the input of a logic gate until the desired change appears at the output of the gate. This is shown in Figure 5. The propagation delay time t_{pd} is the average of the turn-on delay time (t_{PHL}, the output is changing from HIGH to LOW) and the turn-off delay time (t_{PLH}, the output is changing from LOW to HIGH).

$$t_{pd} = \frac{t_{PHL} + t_{PLH}}{2} \tag{11}$$

Note that delay time is measured between the 50% voltage levels.

It is sometimes possible to decrease the propagation delay time of a logic gate by increasing the operating currents of the transistors in the circuit. However, this does increase the power consumption of the gate. The product of propagation delays time and power dissipation ($t_{pd} \times P_{D,av}$) therefore serves as a useful figure of merit on the performance of a gate. Normally a minimum value of the product is desired.

Procedure

1. **Voltage transfer characteristic**

   (a) Set up the circuit shown in Figure 6. Display the voltage transfer characteristics, V_{out} versus V_{in}, using the X-Y mode of the scope. Sketch the result. Note the voltage levels corresponding to V_{OH}, V_{OL}, V_{IL}, and V_{IH}. Using these values, determine the logic swing, the noise margins, and the transition width. Compare these to the calculated values. On your sketch of the scope display, indicate three regions of operation - cutoff, active, and saturation.

   (b) Consider the connection of N similar inverters as load as shown in Figure 7. Let us assume that there are N loading gates which reduce the value of V_{OH} to 1.8V so that the high- and low-level noise margins are equal (NMH = NML = 0.4V). Under this condition, the maximum fan-out can be calculated by solving for N in (9) and is given by

$$N = \frac{R_B(V_{CC} - V_{OH})}{R_C(V_{OH} - V_{BE,sat})} = \frac{8.2\text{k}\Omega(5\text{V} - 1.8\text{V})}{470\Omega(1.8\text{V} - 0.75\text{V})} = 53.17 \rightarrow 53 \qquad (12)$$

   We can simulate this load at the output of Q_0 by using a base resistor $R_{B1} = 8.2\text{k}\Omega/53 = 155\Omega$. Display and sketch the modified transfer characteristic and verify that NMH = NML.

2. **Propagation delay time** (See Figure 8)

   (a) Using a pulse generator as the input, measure the propagation delay time. Sketch the waveform. Increase the frequency of the pulse generator gradually and determine maximum cooperating frequency of the inverter.

   (b) Now add a capacitor across the resistor R_B. Try three different values (C=50pF, 100pF, and 0.01μF) and compare the transient responses of the inverter. Explain the function of the capacitor. Which capacitor value gives the shortest propagation delay?

   (c) Add a germanium diode (1N270) or a Schottky barrier diode across the base and collector terminals as shown in the figure. Explain what happens.

   (d) Calculate the speed-power product for the inverter. The average power dissipation may be calculated by measuring the current from the power supply.

Report

Answer the questions requested in the above procedures.

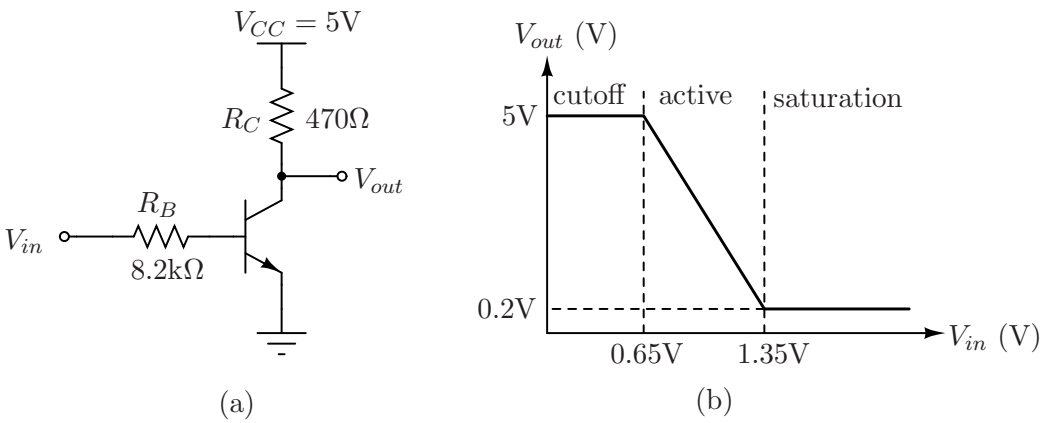


Figure 1: Transistor inverter: (a) circuit diagram, (b) voltage transfer characteristics.

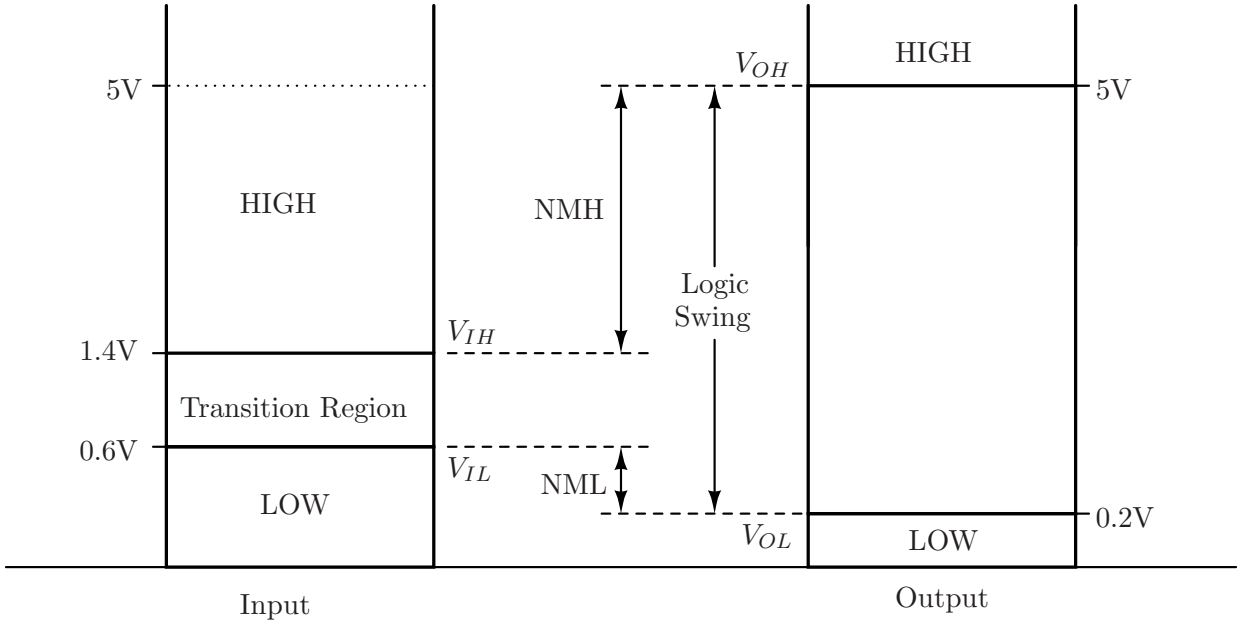


Figure 2: Logic-level diagram showing the noise margins. Threshold voltages are V_{IL}=0.6V, V_{IH}=1.4V, V_{OL}=$V_{CE,sat}$=0.2V and V_{OH}=V_{CC}=5V. Note that the diagram is not to scale.

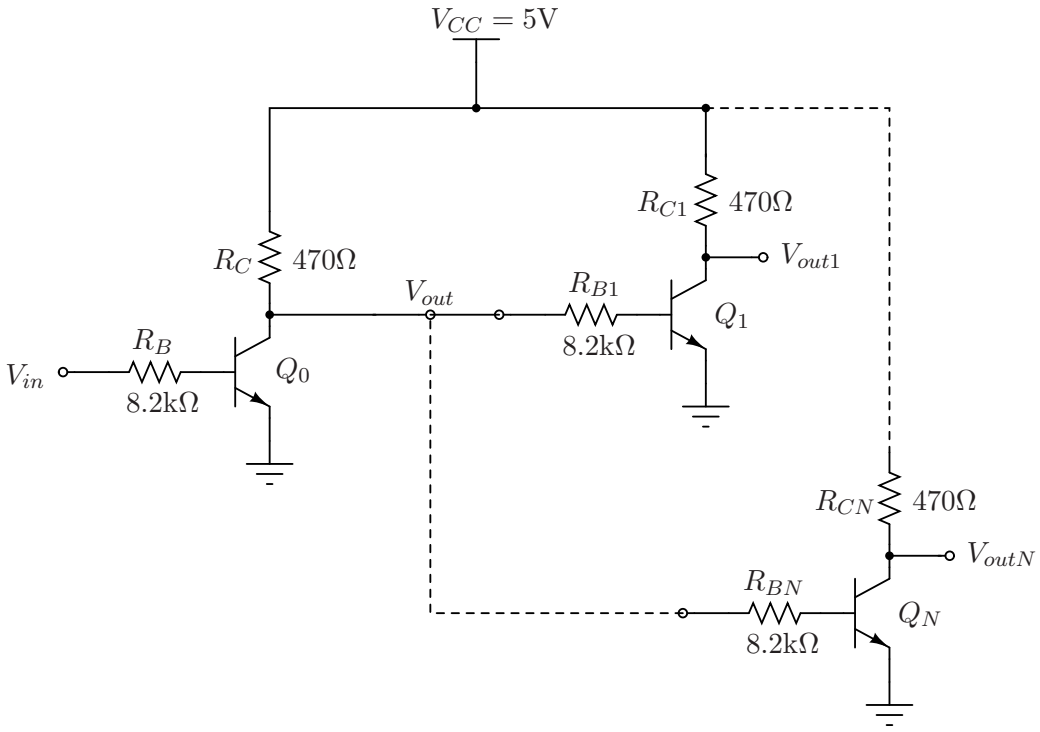


Figure 3: Transistor inverter loaded by N identical inverters.

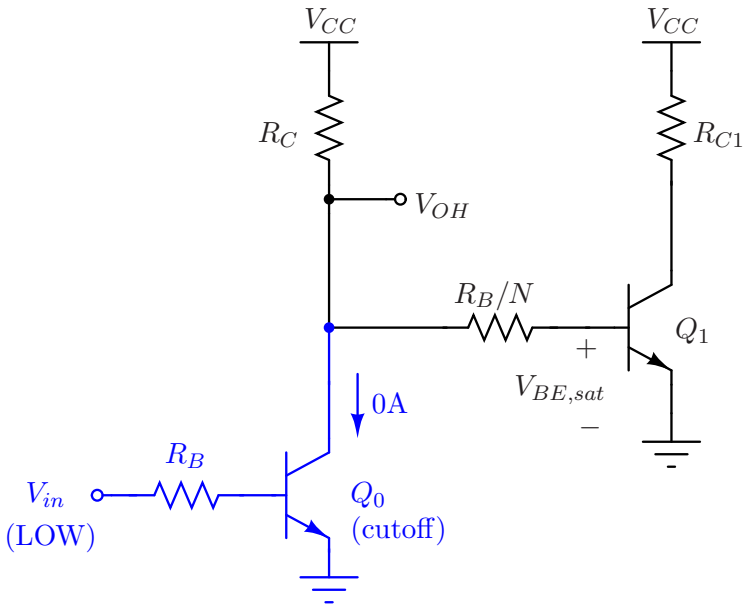


Figure 4: Equivalent circuit for the determination of V_{OH} for an inverter loaded by N identical inverters. Transistor Q_0 can be neglected in the analysis since it is cutoff; therefore all of the current in R_C flows to equivalent resistance RB/N representing the base resistors of the N load gates.

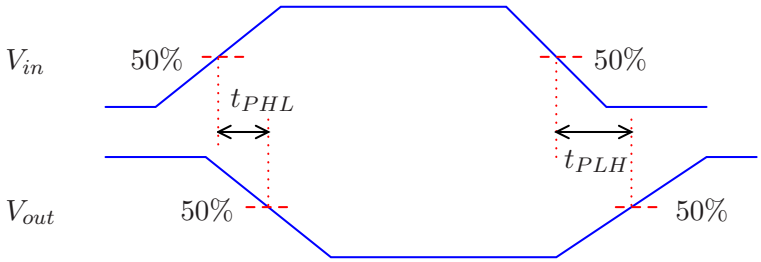


Figure 5: Propagation delay.

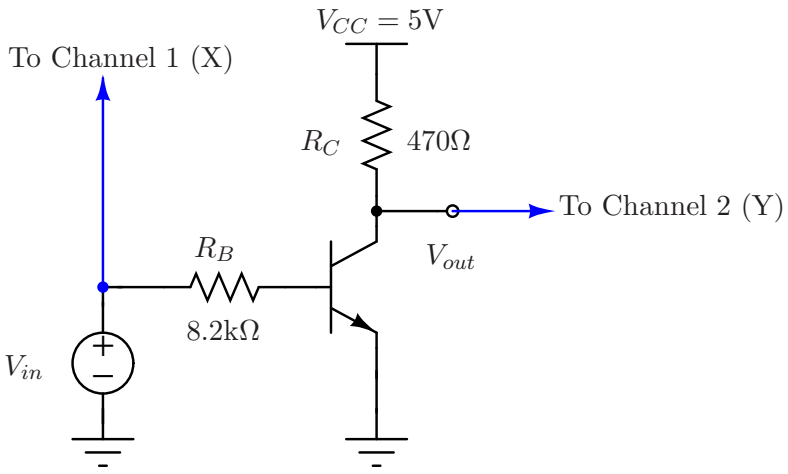


Figure 6: Circuit setup to determine the voltage transfer characteristics of the inverter. The time-varying input voltage should be in the range $0\text{V} \leq V_{in} \leq 5\text{V}$.

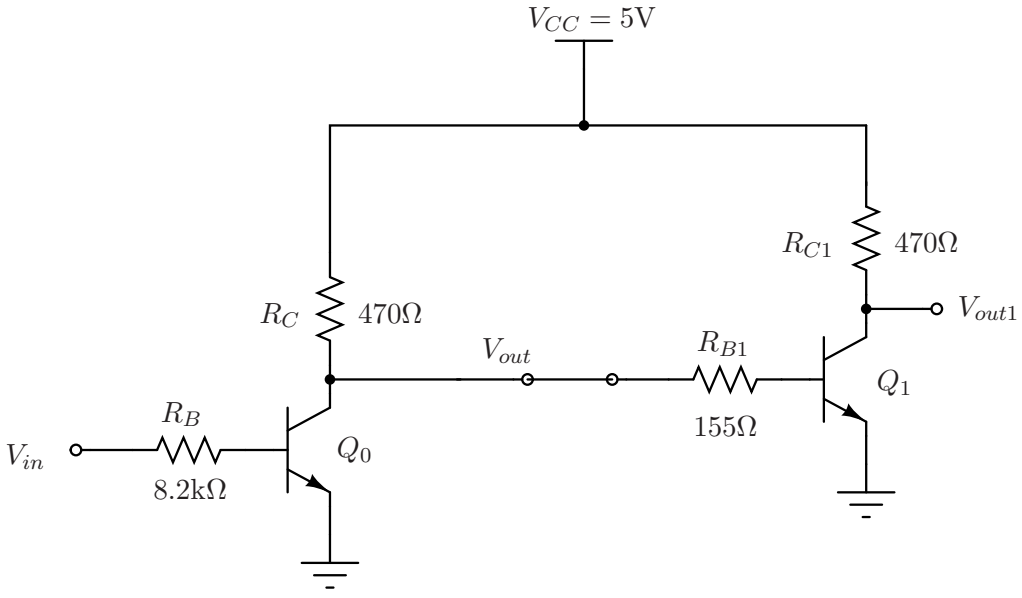


Figure 7: Transistor inverter loaded by an identical inverter. The value of resistor $R_{B1} = R_B/N$ simulates the loading of $N = 53$ inverters at the output of Q_0.

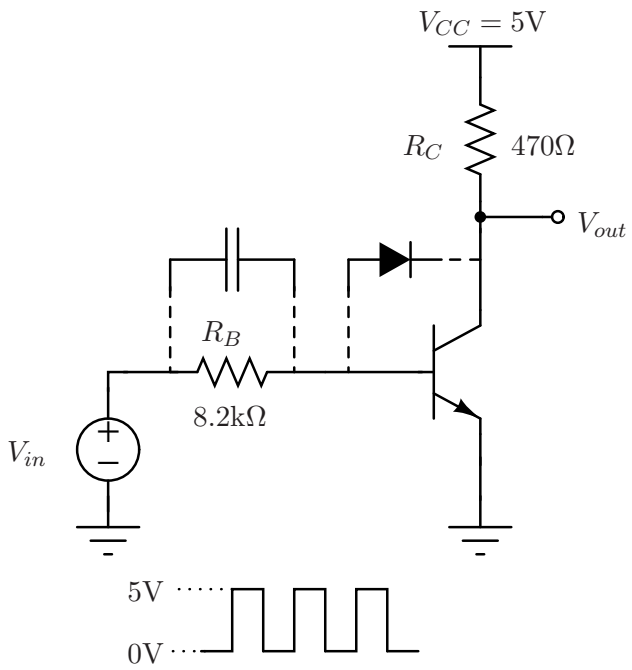


Figure 8: Circuit setup used to determine the propagation delay of the inverter. The capacitor and diode are not part of the initial setup; they are added on to experiment with their effects on the propagation delay and the speed-power product.

Introduction

Be sure to print a copy of Experiment #10 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring regular and semi-log graph paper (cm × cm is best).

Purpose

In this experiment, we will examine the current amplification (A_i), voltage amplification (A_v), input impedance (Z_{in}) and the output impedance (Z_o) of a common-emitter amplifier.

Parts

- 1 - TN3019A NPN transistor
- Assorted resistors and capacitors

Theory

A basic transistor amplifier in the common-emitter configuration is shown in Figure 2. Resistors R_1 and R_2 form a voltage divider across the V_{CC} supply. The function of this network is to provide bias conditions which ensure that the emitter-base junction is operating in the proper region. The AC signal input is added to the bias input through the capacitor C_c. To the AC signal voltage v_s the capacitor behaves approximately as a short circuit to transmit the signal. To the DC bias voltage, the capacitor acts as an open circuit. This decouples the AC source from the DC bias voltage. The emitter resistor R_E is inserted to obtain the desired quiescent emitter current. However, the inclusion of R_E causes a reduction in the amplification. Thus, in many applications the emitter resistor is "bypassed" by a capacitor C_E as shown in the figure.

Preliminary Questions

Use DC analysis techniques to find the DC voltages at the base, collector, and emitter of the transistor. The voltages are referenced to circuit ground. What is $V_{CE,Q}$ and $I_{C,Q}$, the quiescent (dc) values for the operating collector-emitter voltage and the collector current? Assume that current gain $\beta = 100$.

Using the small-signal model for the transistor shown in Figure 1, draw an equivalent small signal circuit model and find the expected values of A_v, A_i, Z_{in} and Z_o. Again, assume $\beta = 100$. The following are the definitions needed for your calculations:

$$A_v = \frac{v_{out}}{v_{in}}, \quad A_i = \frac{i_{out}}{i_{in}}, \quad Z_{in} = \frac{v_{in}}{i_{in}}, \quad Z_{out} = \frac{v_{out}}{i_x}$$

Recall that to calculate the output impedance, the input voltage source must be set to zero and the output terminals must be driven with a test current source of value i_x into the collector connection.

Repeat the above calculations with the emitter bypass capacitor C_E removed.

Procedure

1. Use a 5kΩ variable resistor as R_L. Adjust the value so that it is exactly 500Ω.
2. Construct the amplifier circuit. Determine the Q-point conditions, i.e., measure $I_{C,Q}$ and $V_{CE,Q}$.
3. Adjust v_s so that there is no distortion in the output signal. Measure the ac voltage gain $A_v = v_{out}/v_{in}$ at 50 Hz, 500 Hz, 5 kHz, 50 kHz, and 500 kHz by direct comparison of the v_{out} and v_{in} signals on the scope. Check the voltage phase relationship.
4. Set the generator frequency to 5 kHz. Increase the input signal and determine the maximum peak-to-peak output voltage swing.
5. Measure the ac current gain $A_i = i_{out}/i_{in}$ at the five frequencies. (Note: i_{out} is the current through R_L.) What is the current phase relationship?
6. Determine the ac input impedance Z_{in} at 5 kHz by measuring v_{in} and i_{in} (both ac quantities) and using the relationship $Z_{in} = v_{in}/i_{in}$.
7. Measure the output impedance Z_{out} at 5 kHz using the following procedure. Remove R_L and measure amplitude of the output signal v_{out} (i.e. v_{out} with the load open-circuited). Then place the 5kΩ variable resistor across the output terminals and adjust that resistor until v_{out} becomes 1/2 its original value (i.e. 1/2 the open-circuit voltage). Now, remove the variable resistor and measure its value (which is now Z_{out}) with an ohmmeter.
8. Now remove the emitter bypass capacitor C_E across R_E only. Repeat steps (3) through (7).

Report

1. A_i and A_v vs. frequency should be plotted on semi-log paper.
2. Compare your experimental and analytical values of $V_{CE,Q}$, $I_{C,Q}$, A_v, A_i, Z_{out}, and Z_{in}. Do this for both cases, with and without the emitter bypass capacitor.
3. Comment on the phase relationship of v_{in} and v_{out}. Plot this phase relationship as a function of frequency.

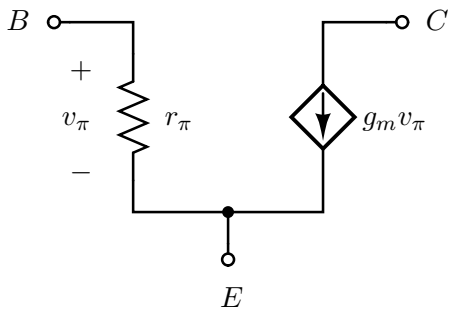


Figure 1: Small-signal model of a bipolar junction transistor. The small-signal parameters can be computed by using the dc operating point values: $g_m = I_C/V_T$, $r_\pi = \beta/g_m$. I_C is the dc value of the collector current and V_T is the thermal voltage which is approximately 26mV at room temperature.

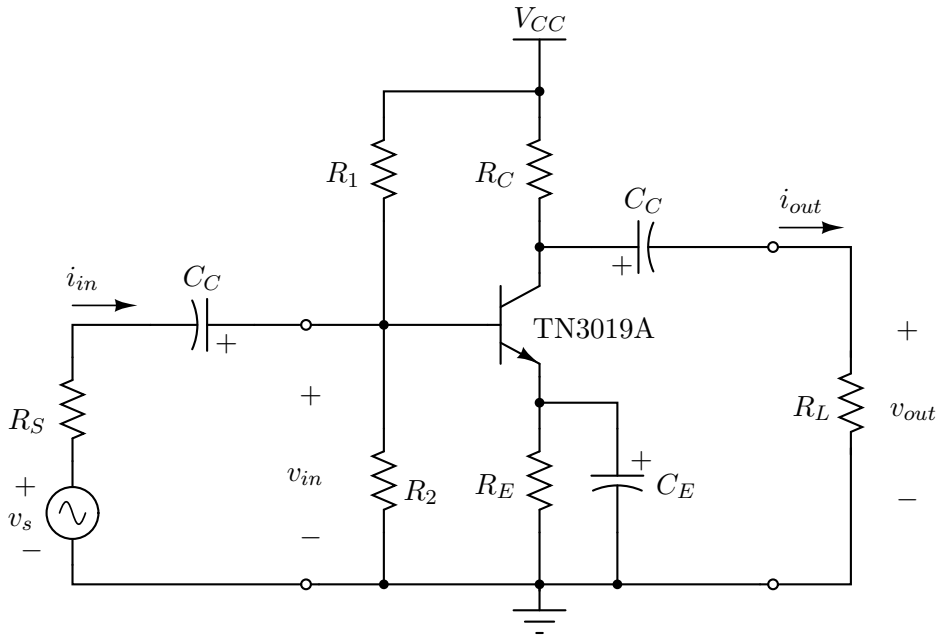


Figure 2: Common-emitter amplifier with coupling capacitors C_C and bypass capacitor C_E. Component values are as follows: $R_S = 100\Omega$ (used to measure i_{in}), $R_1 = 68\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, $R_C = 3.9\text{k}\Omega$, $R_E = 1\text{k}\Omega$, $R_L = 5\text{k}\Omega$ (variable), $C_E = 20\mu\text{F}$, $C_C = 5\mu\text{F}$, $V_{CC} = 30\text{V}$.

Introduction

Be sure to print a copy of Experiment #11 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring regular and semi-log graph paper (cm × cm is best).

Purpose

In this experiment, we will examine the current amplification, A_i, voltage amplification, A_v, input impedance, Z_{in}, and output impedance, Z_{out}, characteristics of a common-collector amplifier.

Parts

- 1 - TN3019A NPN transistor
- Assorted resistors and capacitors

Theory

The common-collector, or emitter-follower, is an extremely useful type of amplifier. The collector is common to both input and output. This is most easily seen in the small-signal equivalent model. Pay close attention to the input and output impedance calculations and measurements.

Preliminary Questions

Use DC analysis techniques to find the DC voltages at the base, collector, and emitter of the transistor. The voltages are referenced to circuit ground. What is $V_{CE,Q}$ and $I_{C,Q}$, the quiescent (dc) values for the operating collector-emitter voltage and the collector current? Assume that current gain $\beta = 100$.

Using the small-signal model for the transistor shown in Figure 1, draw an equivalent small signal circuit model and find the expected values of A_v, A_i, Z_{in} and Z_{out}. Again, assume $\beta = 100$. The following are the definitions needed for your calculations:

$$A_v = \frac{v_{out}}{v_{in}}, \quad A_i = \frac{i_{out}}{i_{in}}, \quad Z_{in} = \frac{v_{in}}{i_{in}}, \quad Z_{out} = \frac{v_{out}}{i_x}$$

Recall that to calculate the output impedance, the input voltage source must be set to zero and the output terminals must be driven with a test current source of value i_x into the collector connection.

Repeat the above calculations with the emitter bypass capacitor C_E removed.

Procedure

1. Use a 5kΩ variable resistor as R_L. Adjust the value so that it is exactly 500Ω.
2. Construct the amplifier circuit. Determine the Q-point conditions, i.e., measure $I_{C,Q}$ and $V_{CE,Q}$.

3. Adjust v_s so that there is no distortion in the output signal. Measure the ac voltage gain $A_v = v_{out}/v_{in}$ at 50 Hz, 500 Hz, 5 kHz, 50 kHz, and 500 kHz by direct comparison of the v_{out} and v_{in} signals on the scope. Check the voltage phase relationship. Please note that the voltage v_{in} taken directly across resistor R_2 and is basically the voltage at the transistor base terminal.

4. Set the generator frequency to 5 kHz. Increase the input signal and determine the maximum peak-to-peak output voltage swing.

5. Measure the ac current gain $A_i = i_{out}/i_{in}$ at the five frequencies. Note that i_{out} is the current through R_L and i_{in} is the current through the 3.3kΩ source resistor. What is the current phase relationship?

6. Determine the ac input impedance Z_{in} at 5 kHz by measuring v_{in} and i_{in} (both ac quantities) and using the relationship $Z_{in} = v_{in}/i_{in}$.

7. Measure the output impedance Z_{out} at 5 kHz using the following procedure. Remove R_L and measure amplitude of the output signal v_{out} (i.e. v_{out} with the load open-circuited). Then place the 5kΩ variable resistor across the output terminals and adjust that resistor until v_{out} becomes 1/2 its original value (i.e. 1/2 the open-circuit voltage). Now, remove the variable resistor and measure its value (which is now Z_{out}) with an ohmmeter.

Report

1. A_i and A_v vs. frequency should be plotted on semi-log paper.

2. Compare your experimental and analytical values of $V_{CE,Q}$, $I_{C,Q}$, A_v, A_i, Z_{out}, and Z_{in}. Do this for both cases, with and without the emitter bypass capacitor.

3. Comment on the phase relationship of v_{in} and v_{out}. Plot this phase relationship as a function of frequency.

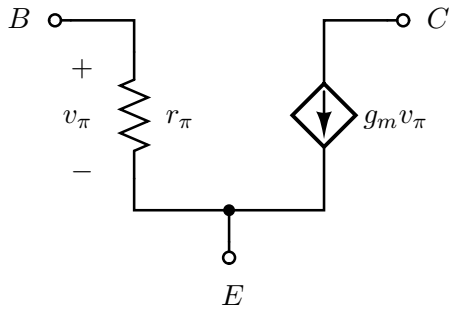


Figure 1: Small-signal model of a bipolar junction transistor. The small-signal parameters can be computed by using the dc operating point values: $g_m = I_C/V_T$, $r_\pi = \beta/g_m$. I_C is the dc value of the collector current and V_T is the thermal voltage which is approximately 26mV at room temperature.

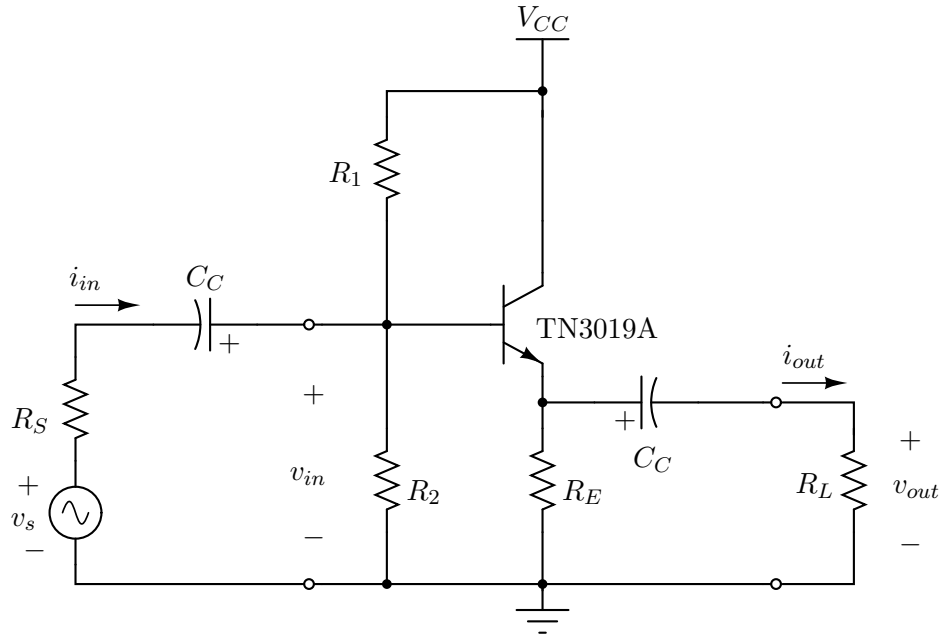


Figure 2: Common-collector amplifier with coupling capacitors C_C. Component values are as follows: $R_S = 3.3\text{k}\Omega$ (used to measure i_{in}), $R_1 = 82\text{k}\Omega$, $R_2 = 68\text{k}\Omega$, $R_E = 3.9\text{k}\Omega$, $R_L = 5\text{k}\Omega$ (variable), $C_C = 5\mu\text{F}$, $V_{CC} = 20\text{V}$.

Introduction

Be sure to print a copy of Experiment #12 and bring it with you to lab. There will not be any experiment copies available in the lab. Also bring graph paper (cm × cm is best).

Purpose

In this experiment you will study the characteristics of a CMOS NAND gate.

Parts

- CD 4011 - CMOS Quad 2-input NAND gate
- 74LS00 - NAND, Quadruple 2 Input

Theory

1. **Basic CMOS Gate** A basic two-input CMOS NOR gate is shown in Figure 1. Q_1 and Q_2 are p-channel MOS transistors, and Q_3 and Q_4 are n-channel MOS transistors. Most CMOS ICs will allow the positive power supply voltage to be set at any value from +3 V to +15 V, depending on the application. The positive power supply and ground are labeled V_{DD} and V_{SS}, respectively, by some manufacturers.

   The basic gate in Figure 1 performs the NOR function as follows. If both inputs are LOW then both Q_1 and Q_2 are on, and both Q_3 and Q_4 are off; the output is HIGH. If at least one input is HIGH, then at least one of Q_1 and Q_2 is off, and at least one of Q_3 and Q_4 is on; the output is LOW. A two-input CMOS NAND gate, shown in Figure 2, reverses the positions of series and parallel transistors to obtain the NAND function.

2. **Logic Levels, Noise Margins, and Fan-out** The input characteristic of a MOS transistor is essentially capacitive, looking like an $10^{12}\Omega$ resistor in parallel with a 5 pF capacitor. Thus the input impedance of a CMOS gate is very high. A CMOS output driving a CMOS input needs to supply almost no current, and hence the voltage drop across its active output transistor(s) is nearly zero. Therefore the logic levels seen in a CMOS system are essentially V_{DD} and ground.

   CMOS circuits typically have a noise immunity of $0.45V_{DD}$. This means that an input which is $0.45V_{DD}$ or less away from V_{DD} or ground will not propagate through the system as an erroneous logic level. This does not mean that the output will be corrected to the proper value of V_{DD} or ground, but it will be closer to correct value than the input was. After passing through a few gates, the error will be attenuated completely.

   CMOS circuits also typically have a DC noise margin of 1 V over the full power supply range. Stated verbally, the specification says that for the output of a circuit to be within $0.1V_{DD}$ of the proper logic level (V_{DD} or ground), the input can be as much as $0.1V_{DD}$ plus 1V away from the proper logic level.

   Since CMOS gates require almost no static input current, the DC fanout of CMOS driving CMOS is virtually unlimited. However, current is required to charge and discharge the

capacitance of CMOS inputs on logic transitions. The propagation delay of a CMOS gate is typically specified for a particular capacitive load, say 50 pF. If the capacitance of the load is higher, the propagation time is longer. As a rule of thumb a designer can assume the load will be 5 pF per CMOS input plus 5 pF to 15 pF for stray wiring capacitance.

Precautions

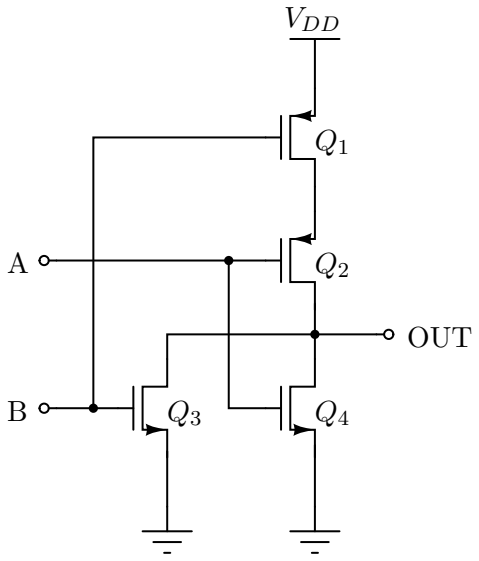
1. While handling 4011 you must be grounded (put your hand on the table which is grounded).
2. The unused input pins of gates must be tied to ground or V_{DD}, what happens if you fail to do this?
3. 4011 chip is kept in a conducting foam piece. Do not keep it anywhere else in your component kit.

Procedure

1. **DC Terminal Characteristics of a 4011 NAND Gate**
   (a) Graph the output voltage versus the input voltage, using a power supply for the input voltage generator, for the range $0 < V_{in} < V_{DD}$ (see Figure 3).
2. **AC Terminal Characteristics of a 4011 NAND Gate** (see Figure 4)
   (a) Using a pulse generator as the input, measure the rise time, fall time, and propagation delay of the 4011. Are the HIGH-to-LOW and the LOW-to-HIGH propagation delays the same? Explain. Are the rise and fall times the same? Explain.
   (b) Now attach a 100 pF capacitor to the output of the 4011 with the other lead at ground. What are the rise and fall times now? If the input capacitance of a 4011 gate were 5 pF, what maximum fan-out would you use in a CMOS system before deciding to buffer a signal to drive more gates?
   (c) Construct the circuit shown in Figure 5. What waveform do you observe on the scope?
   (d) Construct the circuit shown in Figure 6. With the pulse generator set to 0 to 5 V square waves, sketch the waveforms at points A, B, and C. Repeat the above for a 2 V square wave. Gradually increase the square-wave until you find the threshold voltage V_{IH} for the 4011.

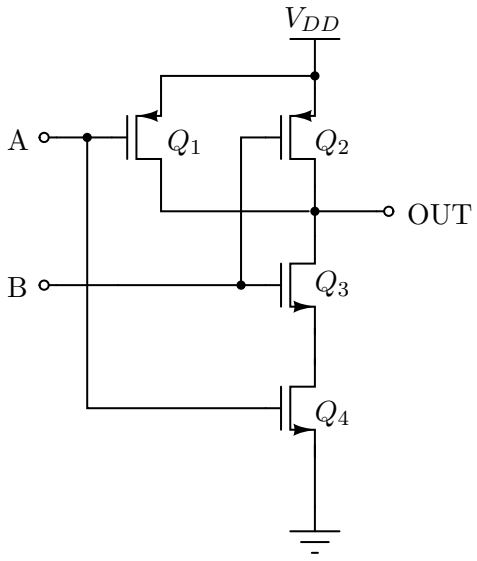
Report

In your report, include the recorded plots and answers to the questions from the experimental procedure.



A	B	Q_1	Q_2	Q_3	Q_4	OUT
0	0	short	short	open	open	high
0	1	open	short	short	open	low
1	0	short	open	open	short	low
1	1	open	open	short	short	low

Figure 1: CMOS NOR gate and corresponding truth table. Q_1 and Q_2 are p-channel MOSFETs while Q_3 and Q_4 are n-channel MOSFETs.



A	B	Q_1	Q_2	Q_3	Q_4	OUT
0	0	short	short	open	open	high
0	1	short	open	short	open	high
1	0	open	short	open	short	high
1	1	open	open	short	short	low

Figure 2: CMOS NAND gate and corresponding truth table. Q_1 and Q_2 are p-channel MOSFETs while Q_3 and Q_4 are n-channel MOSFETs.

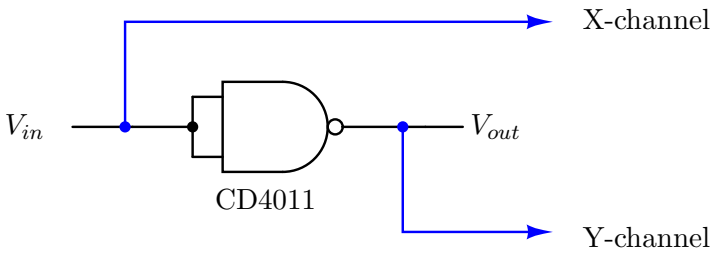


Figure 3: Circuit used to determine the dc characteristics of a CD4011 CMOS NAND gate. The power supply voltage V_{DD} = 5V, 10V, 15V.

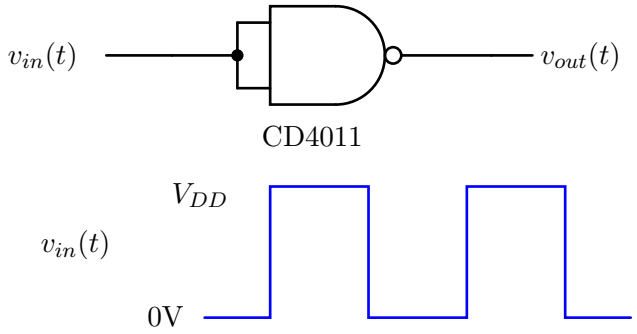


Figure 4: Circuit used to determine the ac characteristics of a CD4011 CMOS NAND gate. The power supply voltage $V_{DD} = 5\text{V}$, 10V, 15V.

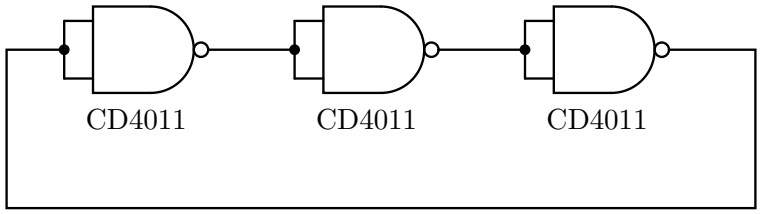


Figure 5: Circuit used to determine the ac characteristics of a CD4011 CMOS NAND gate. The power supply voltage $V_{DD} = 5\text{V}$.

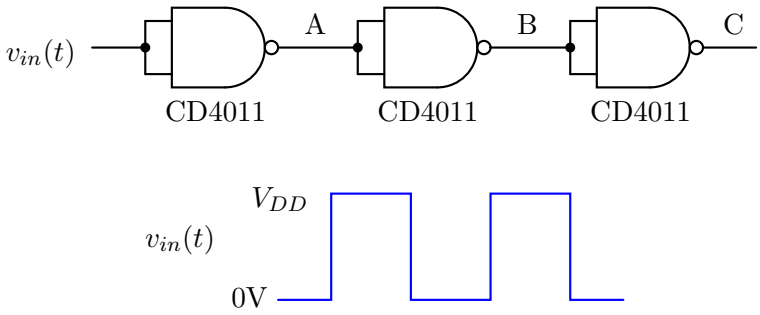


Figure 6: Circuit used to determine the ac characteristics of a CD4011 CMOS NAND gate. The power supply voltage $V_{DD} = 5\text{V}$.