ECE 342 : EXPERIMENT I Week 2
A SIMPLE R-C CIRCUIT

Purpose:
In this experiment you will learn how to measure the magnitude and phase of the sinusoidal steady-state frequency response of a simple circuit. From this data you will plot these responses on semi-log paper. In examining this circuit you will also become familiar with the test equipment that is used in this laboratory.

Parts:
None

Theory:
The sinusoidal steady-state transfer function of an analog electronic circuit is very important in analyzing the evaluating that system. The circuit is excited by a sinusoidal source. The transfer function is the ratio of the response (current or voltage) at one location in the circuit to the response at another location in circuit. The ratio of the response magnitudes, which is usually given in decibels and is defined below, is found as a function of frequency. The phase difference of the responses is found as a function of frequency.

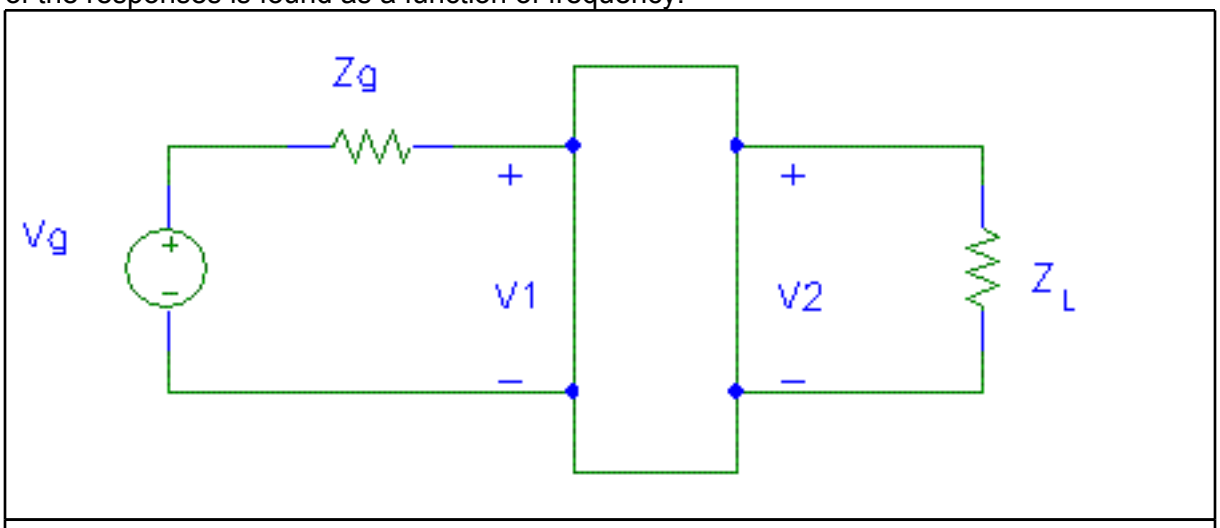


Figure 1

To make this more specific consider the diagram shown in figure 1. Here the responses will be sinusoidal voltages represented as phasors, V1 and V2. Recall that these are complex quantities that are functions of the excitation frequency, w . As complex quantities these may be expressed as a magnitude, |V|, and phase, V. We can now define the sinusoidal steady-state transfer function as

$$H(\omega) = \frac{V_2(\omega)}{V_1(\omega)}$$

What is usually plotted (on semi-log paper) are the following two quantities:

$$|H(\omega)|\,(\text{in dB}) = 20\log\left[\frac{|V_2(\omega)|}{|V_1(\omega)|}\right] \qquad \theta(\omega) = \angle V_2(\omega) - \angle V_1(\omega)$$

The voltages measured in the circuit are sinusoids and displayed on the oscilloscope. Both voltage magnitudes used in the above formula can be either maximum values, peak-to-peak values, or RMS values. The phase difference is easily measured using a dual trace oscilloscope. Display both signals, V1 and V2, on scope screen with the baselines (ground) on the same line. Trigger the scope on the signal, V2. The method of determining the phase difference, q(w), is shown in figure 2.

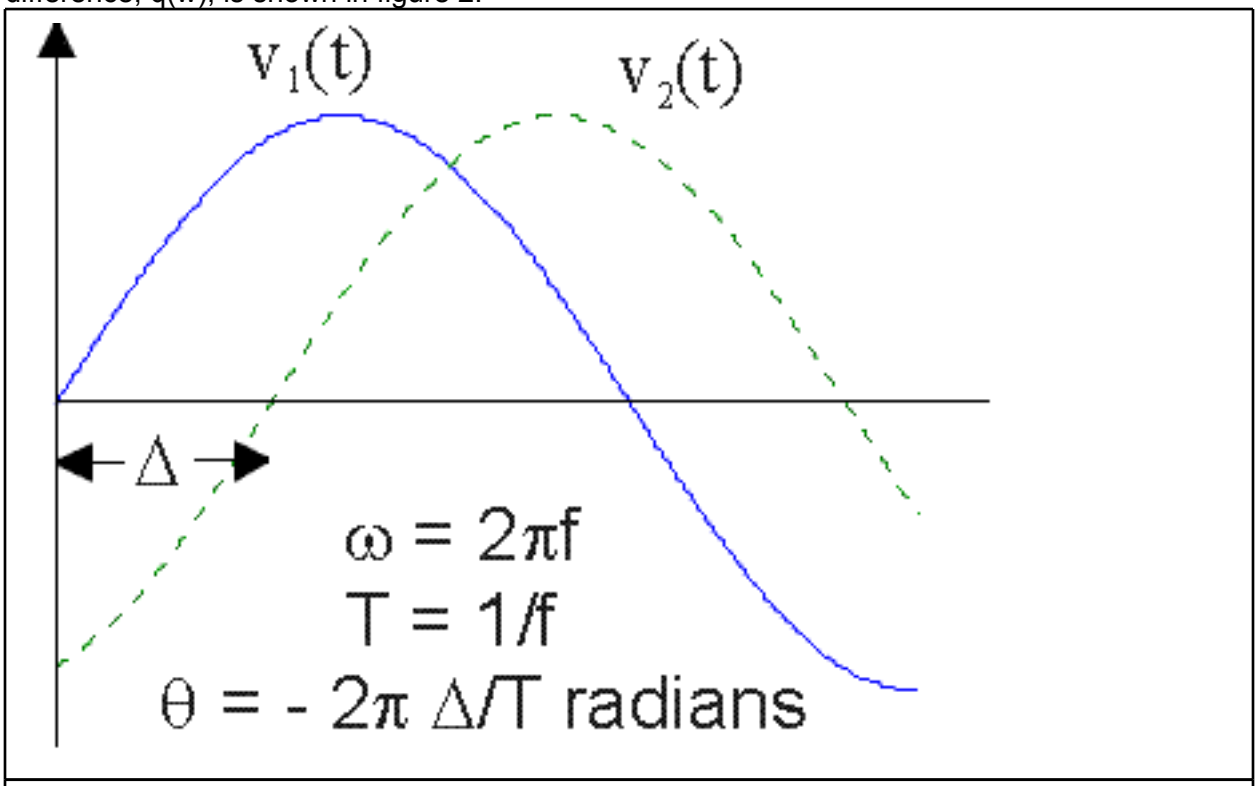
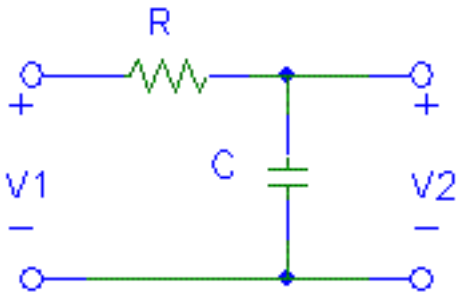


Figure 2

Procedure:

1. Set up the circuit shown in figure 3.



R = 1.59 kΩ
C = 10 nF

Figure 3

2. Measure |V1|, |V2|, and q for a number of different e.g. 0.1 KHz, 0.5 KHz, 1.0 KHz, 5.0 KHz, 10 KHz, 50 KHz, 100 KHz, 500 KHz, and 1 MHz.
3. Plot |H(f)| (in dB) and q (f) on 5-cycle semi-log paper.

Questions:

Construct an "exact" Bode plot for |H(f)| and q (f) for the circuit shown in figure 3. How does it

compare with the plot from procedure #3? Explain the source of possible discrepancies?

ECE 342: EXPERIMENT II Week 3
SINGLE SUPPLY BIASED INVERTING AC AMPLIFIER

Contents

Purpose:

The purpose of this experiment is to demonstrate (1) the effect of varying the bias resistors on the quiescent DC output voltage, and (2) the operation of an AC inverting amplifier powered by a single supply voltage.

Theory:

Schematic of Circuit:

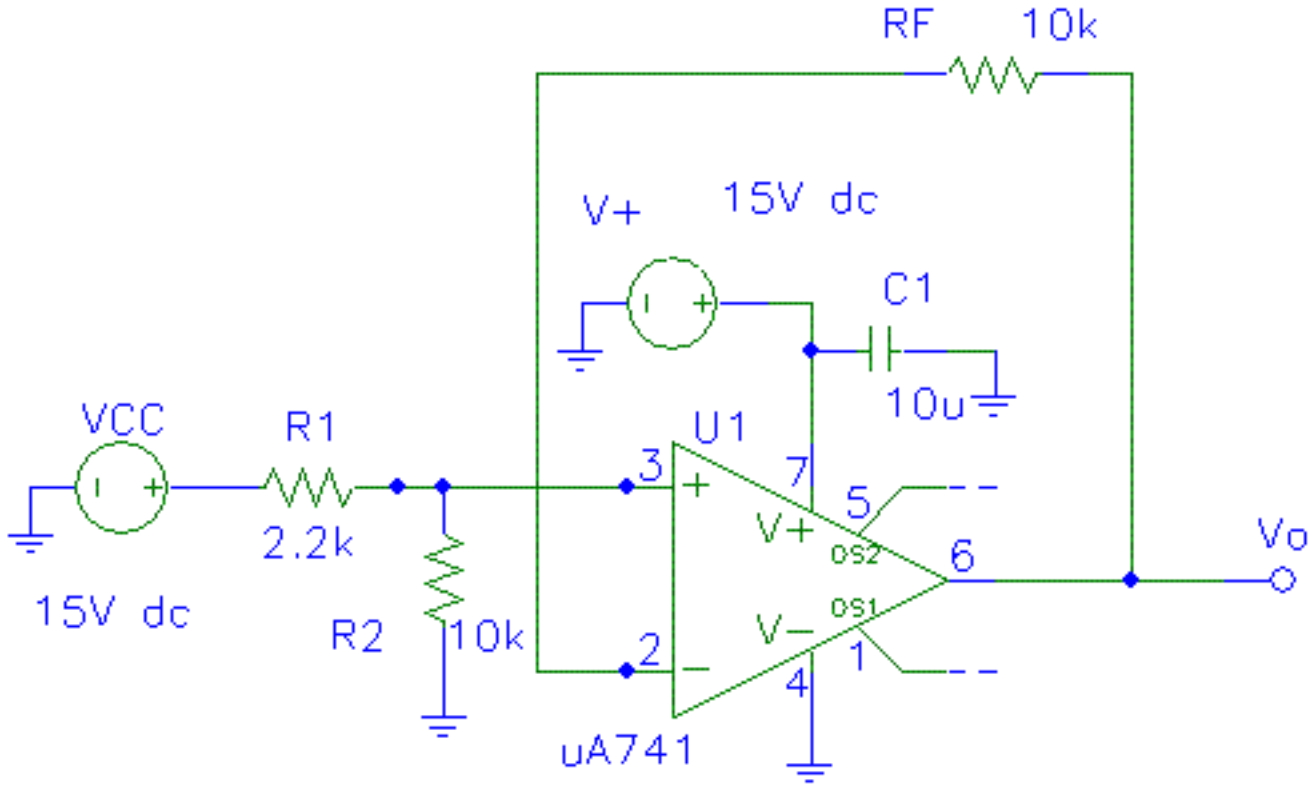


Figure 1. Biasing circuit

Formulas:

Quiescent DC output voltage

$$V_O(\text{DC}) = \left(\frac{R_2}{R_1 + R}\right)V_{CC}$$ (Eq. 1)

Usually,

$$V_O(\text{DC}) = \frac{V_{CC}}{2}$$

when R2 = R1.

Inverting amplifier

Closed-loop voltage gain

$$A_{CL} = -\frac{R_F}{R_1} \quad (180^\circ \text{ phaseshift})$$ (Eq. 2)

Coupling capacitors (low-frequency response)

$$C_1 = \frac{1}{2\pi f_c R_1}$$ (Eq. 3) and, $$C_2 = \frac{1}{2\pi f_c R_L}$$ (Eq. 4)

Procedure:

1. Wire the circuit shown in the schematic of Figure 1 and apply power to the breadboard. Make sure that pin 4 of the op-amp is now connected to ground. With your DC voltmeter, measure the power supply voltage (VCC) and record this value in Table 1. Using this value and the resistors values in Eq. 1, calculate the expected DC output voltages and record them in the last column of the table.

Table 1

Supply Voltage (VCC)			
R1	Measured VB	Measured Vo	Expected Vo
2.2 kΩ			
6.8 kΩ			
10 kΩ			
33 kΩ			
68 kΩ			

2. Separately measure the DC voltages at pins 3 (VB) and 6 (Vo) of the op-amp with respect to ground and record these values in Table 1.

3. Vary resistor R1 to the four remaining values given in Table 1. Each time you change R1, first turn off and disconnect the power from the breadboard. Record each measured value and compare it with the expected value (Eq. 1). At what resistance value is the DC output voltage approximately one-half the supply voltage measured in Step 1?

You should find that the quiescent output voltage is one-half the supply voltage when R1=R2, or 10 kΩ. In general, for proper operation from a single supply voltage, the quiescent DC output voltage is made equal to one-half the supply voltage.

4. Turn off and disconnect the power from the breadboard and wire the inverting amplifier circuit shown in Figure 2. Set your oscilloscope to the following approximate settings:

- Channels 1 and 2: 0.1 V/division, DC coupling
- Time base: 0.2 ms/division

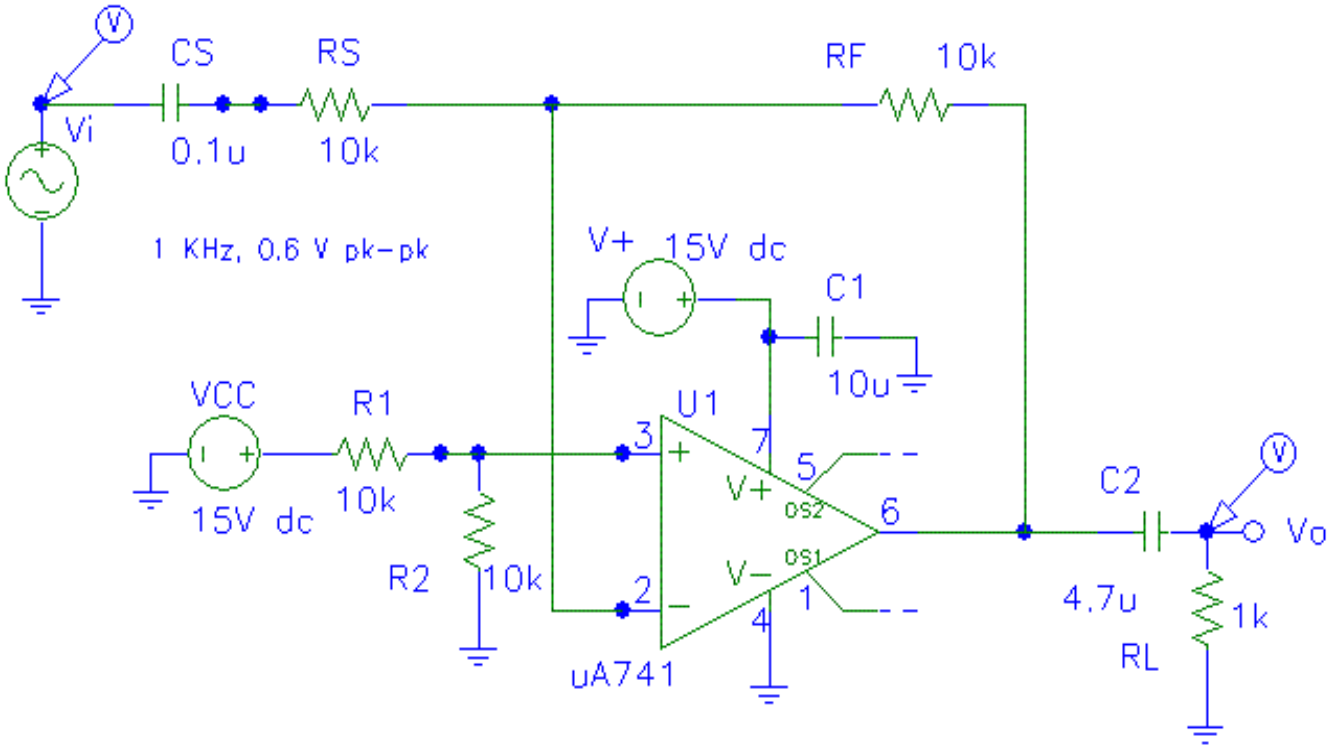


Fig. 2. Single supply inverting amplifier.

5. Apply power to the breadboard and adjust the input signal at 0.6 V peak-to-peak and its frequency to 1 kHz. Is there any difference between the amplifier's input and output signals? You should observe that the output amplitude is the same as the input although it is 180o out of phase with the input.

6. Measure the peak-to-peak output voltage and calculate the voltage gain. Record these values in the first row of Table 2 and compare them with the expected values (Eq. 2). You should calculate a closed-loop voltage gain of 1, since both signals are the same voltage.

Table 2

RF	Measured Vo	Measured Gain	Expected Gain
10 kΩ			
100 kΩ			

7. Now transfer the Channel 2 probe to the output pin of the op-amp (pin 6). Are there any differences between the output signal at pin 6 and the output signal across the 1-kΩ load? You should have observed that (1) the amplitude of both signals is the same, and (2) that both

signals are each 180o out of phase with the input signal. Most importantly, however, the output signal at pin 6 of the op-amp is approximately one-half the supply voltage higher than the signal across the load. This is because the output coupling capacitor (C2) AC couples the signal at the output of the op-amp to the load removing the DC quiescent voltage.

8. Keeping the input signal constant at 0.6 V, change resistor RF to the 100 kΩ value given in Table 2. Determine the amplifier's closed-loop voltage gain and compare each value with the expected value (Eq. 2). Record all results in the table.

9. Set Rf = 100 kΩ and channel 2 probe as in Fig. 2. Set the i/p frequency to 1 kHz and vary the i/p magnitude from 0.4v to 1.4 volts peak to peak in steps of 0.2 volt. Measure the o/p magnitude at each step and fill the table 3. Graph the o/p as a function of the i/p magnitude. Is the output directly proportional to the input (linear amplifier)? Explain.

Table 3

Vi[v]	Vo[v]	GAIN
0.4		
0.6		
0.8		
1.0		
1.2		
1.5		

10. Measure the frequency response between the 3 dB points. With Rf = 100 kW , set the i/p to 0.2 volts and vary the frequency observing where the o/p remains approximately constant (with constant i/p voltage). This is the midrange. Choose one frequency approximately in the middle of the midrange and record the signal values in the 3rd row of table 4.

Table 4

	Frequency	Vi[v]	Vo[v]	GAIN
1				
2				
3				
4				
5				

Decrease the frequency up to the point that the gain drops 3 dB below the midrange value. Record the values in the 2nd row of table 4. Take the values for the 1st row at a frequency approximately 10 times lower. Now increase the frequency beyond the midrange value, up to the point that the gain again drops 3 dB below the midrange. Fill row 4. Use a higher frequency

for row 5. (Can you go to the frequency at which the gain is 1 to determine the unity gain bandwidth?) Repeat this frequency scan for i/p equal to 1.0 v peak to peak. Graph the response in dB as a function of frequency for the 2 different input curves. Interpret the curves, and explain any differences between the curves.

ECE - 342 EXPERIMENT III Week 4
NON IDEALITIES OF OP AMPS

Purpose:
To measure non-ideal dc input effects, i.e., Input Offset Voltage, Input Bias Current and Input Offset Current (part A) and to measure slew rate (part B).

Parts:
741 Operational Amplifier
10 kW Potentiometer

Theory:
Figure 1 shows a model of a non-ideal op-amp.

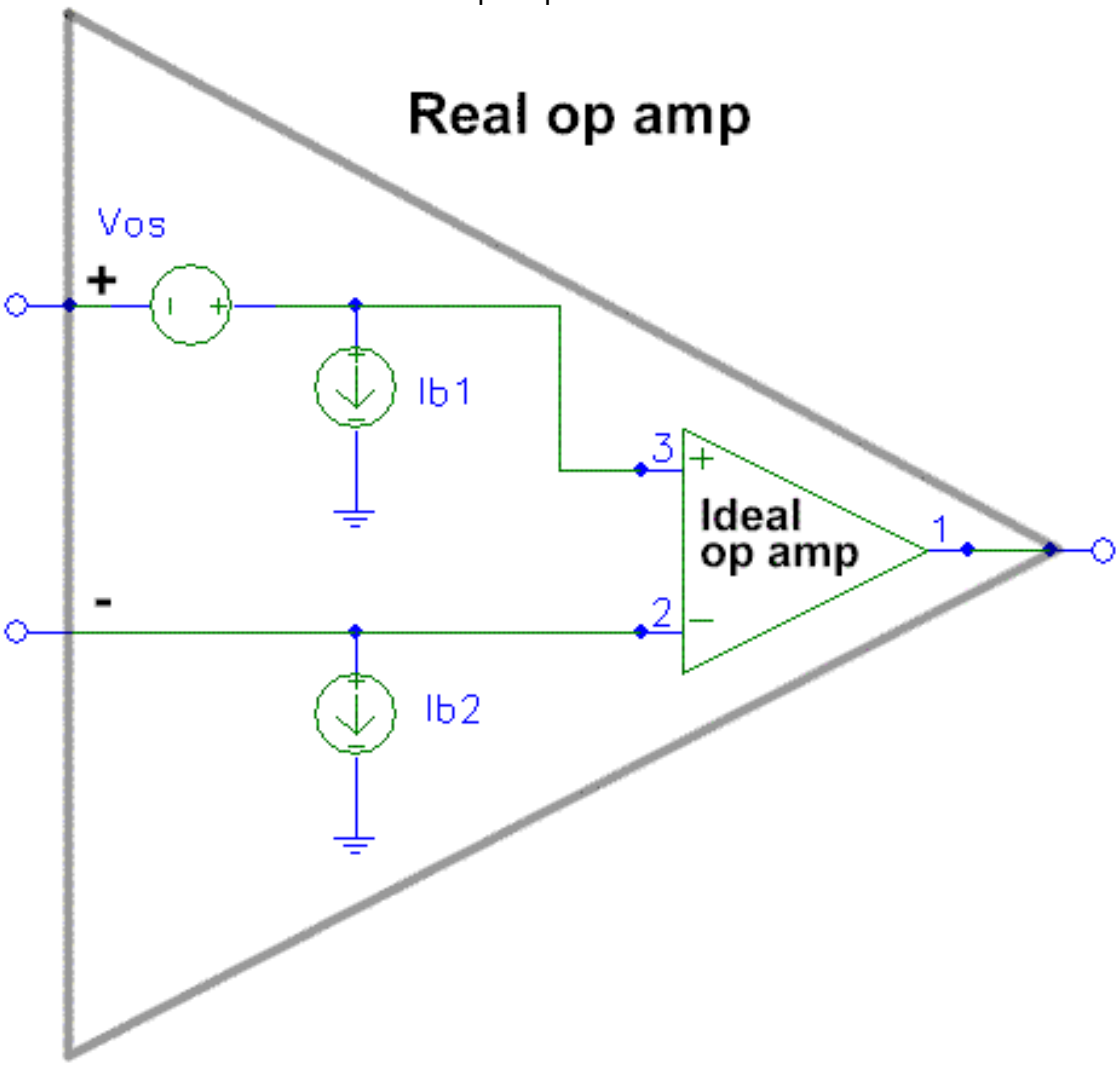


Figure 1.

$$I_{bias} = \frac{I_{b1} + I_{b2}}{2} \qquad I_{os} = \left| I_{b1} - I_{b2} \right|$$ and

Procedure:
Part A - Input Offset Voltage, Input Bias Current and Input Offset Current
1. First, assemble the circuit as shown in figure 2. Use ±15V power supplies. Measure VO ,

the output voltage at the output of the op amp. Calculate VOS. Explain why you can practically ignore both input currents Ib2 and Ib1 for this calculation.

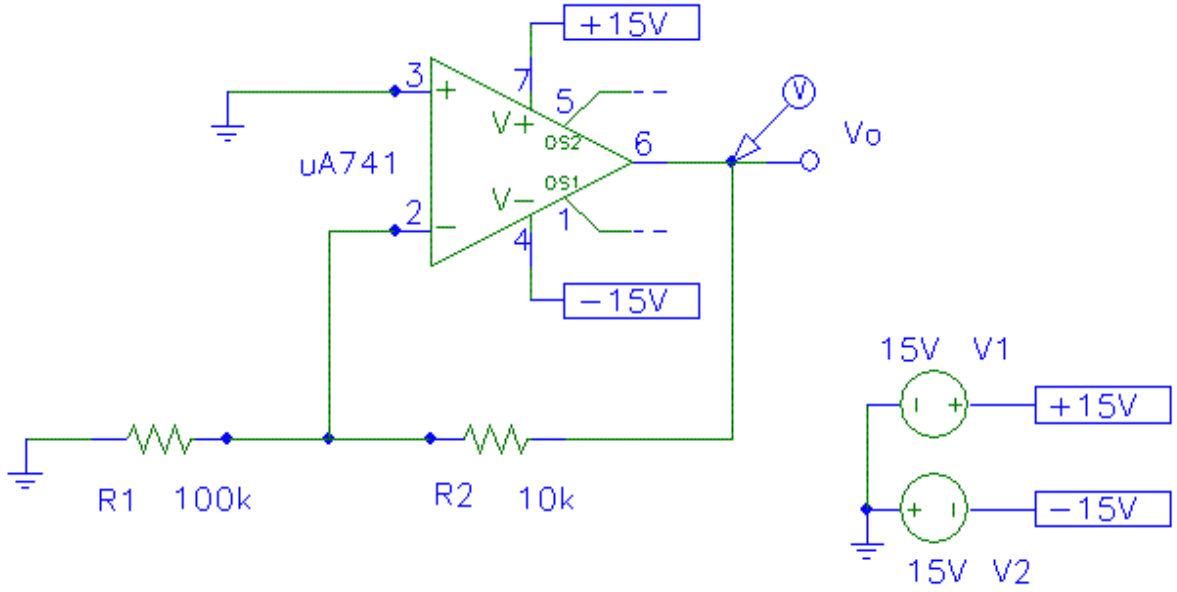


Figure 2.

2. Now assemble the circuit in Fig. 3, *carefully record the actual values of the resistances*. Short-circuit R-, R+ and Ra and check that you have the same output as in step 1.

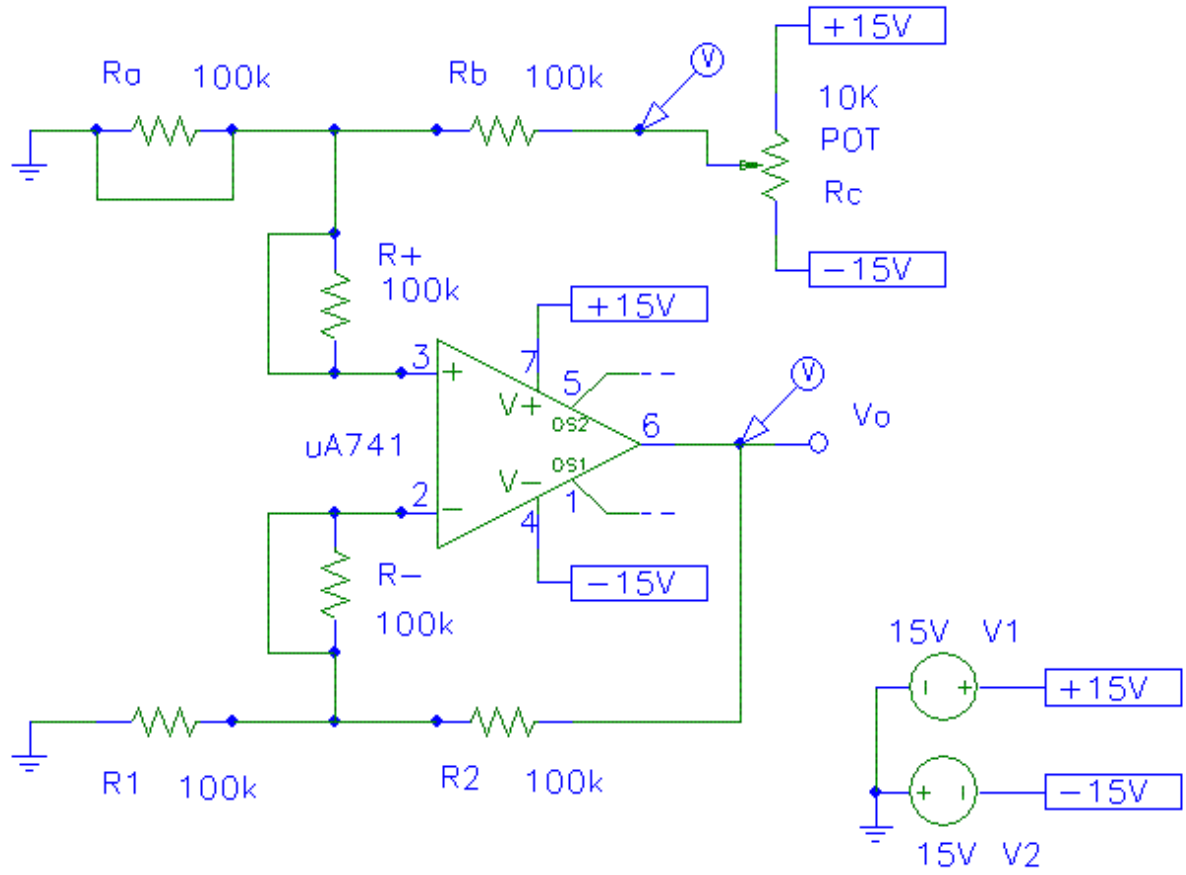


Figure 3.

3. Remove the short-circuit from Ra. Adjust potentiometer Rc until VO , the output voltage at the output of the op amp is zero volts (you will then keep this adjustment). Measure the voltage on the sliding terminal of the potentiometer and calculate the offset voltage VOS that has been compensated. Does this result agree with the one in step 1?

4. Short-circuit Ra and remove the short-circuit from R-. Explain what has changed from the circuit in Fig. 2. Measure VO , the output voltage at the output of the op amp. Calculate the input offset current corresponding to the bias current Ib2. Carefully explain how VOS and Ib2 contribute to VO , the output voltage of the op amp.

5. Finally remove the short-circuit from both Ra and R+ and short-circuit R-. Measure the voltage the output of the op amp, VO. Estimate the input offset current. Readjust the potentiometer Rc until VO is zero once again. Measure the voltage on the sliding terminal of the potentiometer and use this and the value of this voltage after the first adjustment to provide a second estimate of the offset current.

Part B - Slew Rate

1. First, assemble the circuit as shown in Fig. 4 to measure the slew rate. Use ±15V power supplies. Take one 1kW resistor and one 10kW resistor. Measure their actual resistances and record them.

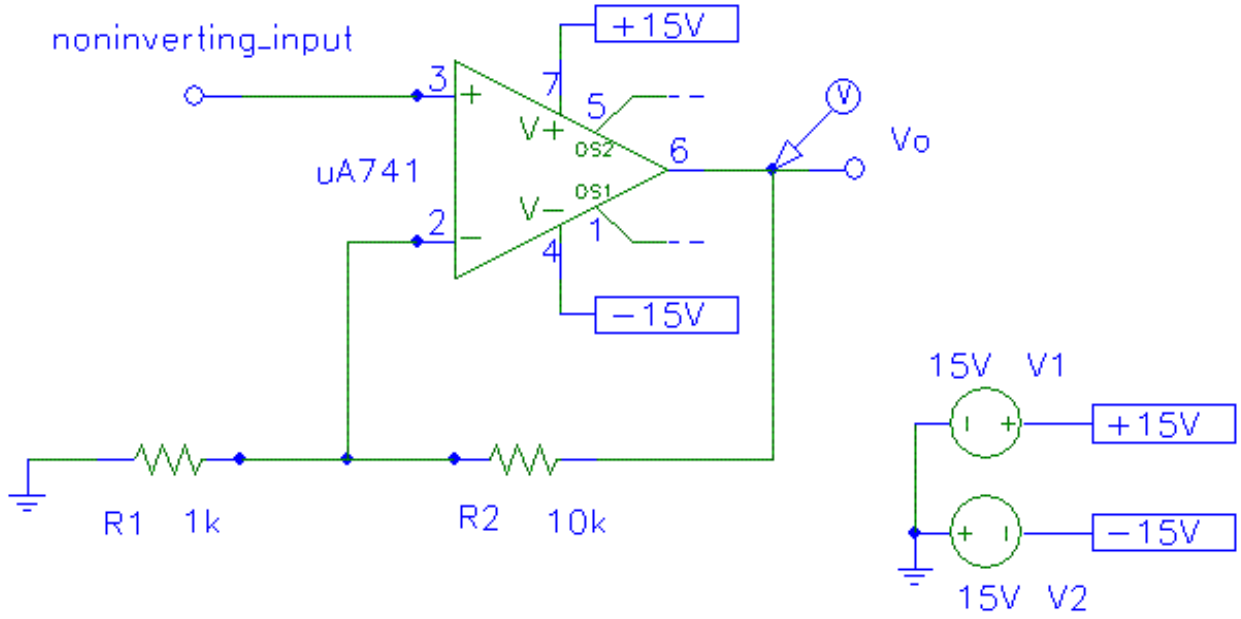


Figure 4.

2. Apply a 100mV pk-pk square wave at 1kHz to the noninverting input of the op amp.

3. Observe the waveform at the output of the op amp. Do you observe slew rate?

4. Now raise the input voltage by a factor of two. Estimate the slew rate. Raise the input voltage once again by a factor of two. Estimate slew rate again. Explain the changes at the observed output voltage. Lower back the input voltage until the slew rate disappears. Can you calculate that voltage level in advance, using the previously estimated slew rate? Check the consistency of your calculation and the actual required voltage level.

5. Apply a 2.5V pk-pk sine wave at 20 kHz. Explain the waveform at the output. Record the ratio of output peak-to-peak voltage versus the input peak-to-peak voltage. Can you call this number *the gain at 20 kHz?*

6. Apply half of the previous input voltage. Record the ratio of output peak-to-peak voltage versus input peak-to-peak voltage. Is this lower or higher than the previous one? Explain

why. Estimate the frequency needed to observe the same ratio as in section (5). Increase the frequency of the input signal until the ratio of the output peak-to-peak voltage versus input peak-to-peak voltage become the same as in section (5). Record the value of this frequency. Is this value consistent with your estimate?

Report:

Include answers and explanations in your report.

ECE - 342 EXPERIMENT IV Week 6
DIFFERENTIAL AMPLIFIER

Purpose:
Familiarization with biasing, common-mode gain, differential-mode gain, and transfer characteristics of a differential amplifier.

Parts:
CA 3086 Transistor Array

Theory:
1. Introduction
The differential transistor pair (see figure 3) coupled at the emitters via a constant current source has a number of applications chief among these is the input stage of integrated circuit operational amplifier. The major advantage of this type of circuit is its high differential voltage gain and low common mode gain. Basically, the differential pair steers the emitter current, I, between the two transistors, Q1 and Q2. If vB1 > vB2, then iC1 > iC2, but iC1 + iC2 » I. If vB2 > vB1, then iC2 > iC1, but iC1 + iC2 » I. A difference of about 200 mV between base voltages will cause all of the current, I, to flow through only one of the transistors.
The current, IE is set by the constant current source of Q3. I is determined by R1, R2, RE and VEE, using the following approximation

$$I = \alpha \left[\left(\frac{-V_{EE} R_2}{R_1 + R_2} \right) - 0.7 \right] / R_E$$

2. Preliminary Questions (NEED TO BE DONE BEFORE THE LAB SESSION)
[A]. Common Mode Gain

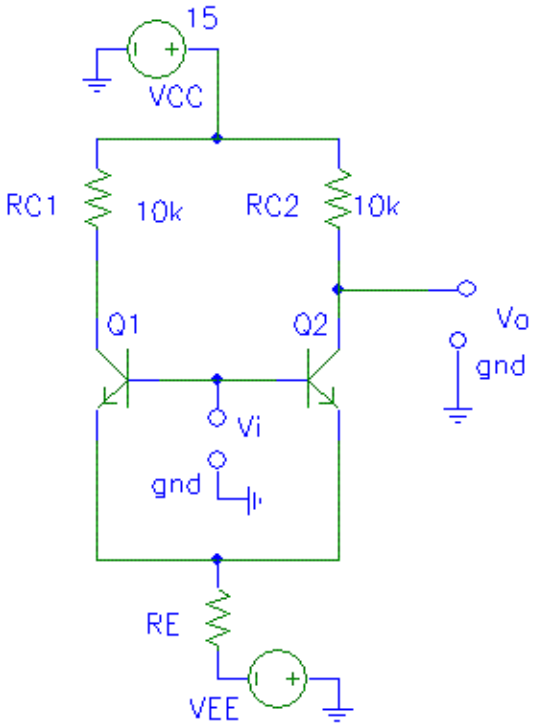


Figure 1
The differential amplifier configurations are to be designed, for a quiescent output voltage of 5 V.
1. For the circuit of figure 1 obtain an expression for the common mode voltage gain.
2. GIVEN b = 100, VC = 5 V, and RE = 1 kW calculate the common mode gain and the required value of VEE. Repeat the calculation for RE = 10 kW . (HINT: USE HALF CIRCUIT ANALYSIS, THEN D vB = 0.)

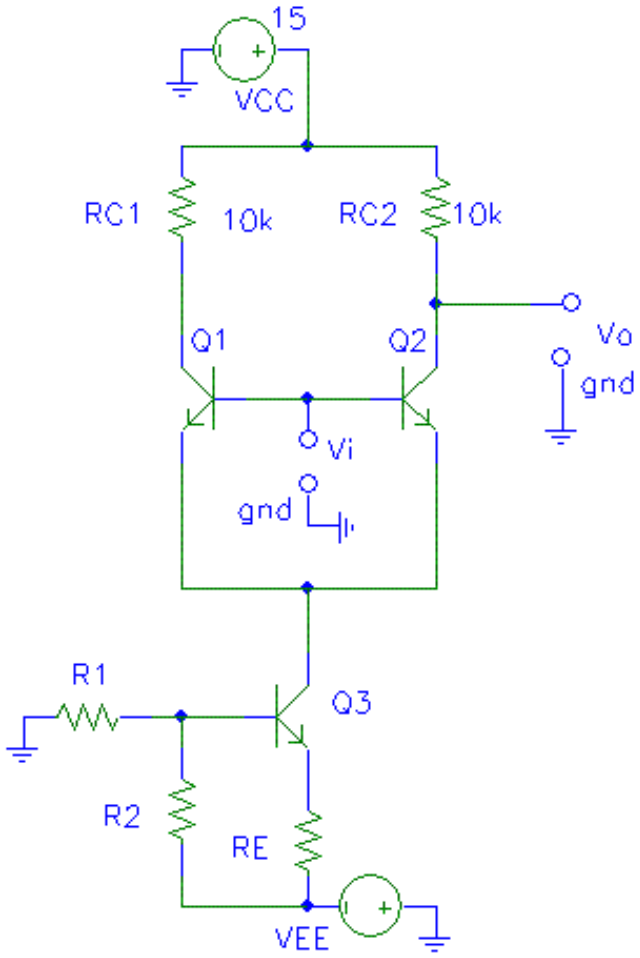


Figure 2
1. VEE = -10 volts. If RE is (a) 1 kW or (b) 4 kW assuming very small base current for Q3 in figure 2, choose two suitable sets of values for R1, R2. Make sure that the current through R1 and R2 is 1 mA or higher.
2. Calculate the quiescent value of VCE3 for both values of RE chosen in question 3. (HINT: USE HALF CIRCUIT ANALYSIS, THEN vB = 0.)
3. The maximum instantaneous common mode voltage which may be applied to the differential amplifier of figure 2 is limited by the saturation on Q1 and Q2. The minimum common mode voltage is limited by the saturation of Q3. Calculate the allowed common mode voltage range for both values of RE chosen in question 3. Assume vCE (SAT) = 0.2 V and vBE (SAT) = 0.7 V. The minimum (most negative) common mode voltage may also be limited by the fact that VC cannot go higher than VCC. For large common mode gain this may happen before Q3 saturates.
4. Obtain an expression for the effective ac resistance looking into the collector of Q3, and then use this resistance to calculate the common mode gain for both sets of resistor values chosen in

question 3. Assume rO = 64.1 kW .

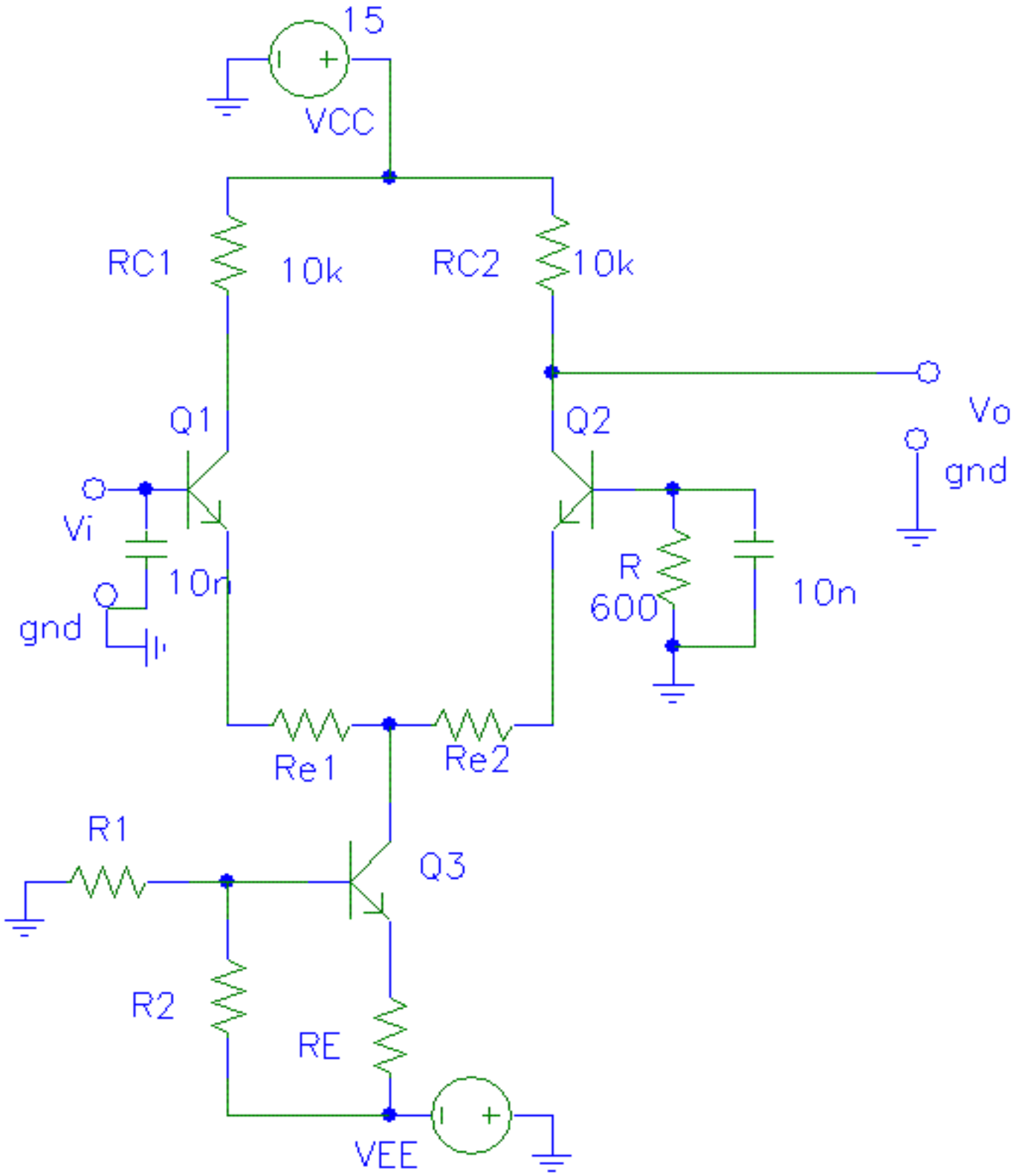


Figure 3
[B]. Differential Voltage Gain

1. The differential amplifier is often operated with a signal applied to one input and the other input connected to a resistor which is grounded. This is called the single-ended mode. The single-ended voltage gain is approximately equal to the difference mode voltage gain. What is the minimum value of the common mode rejection ratio if the approximation is to have a maximum of one percent error? This result provides a convenient method for measuring the difference mode gain.
2. Show that the difference mode voltage gain of figure 3 with Re = 0 is

$$|A_d| = g_m R_C = \frac{\alpha I R_C}{2V_T} \approx \frac{I R_C}{2V_T}$$

and with Re ¹ 0 is

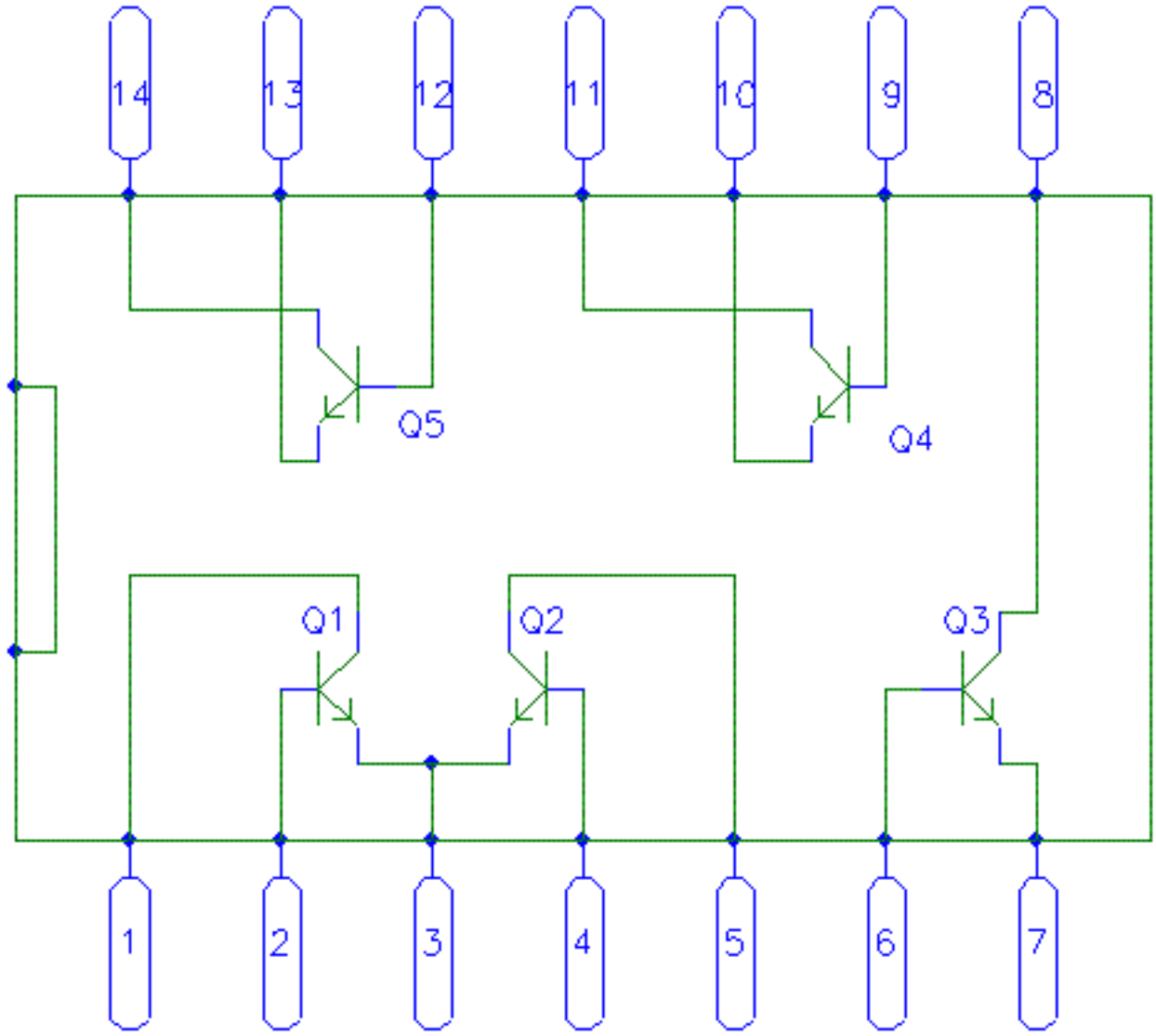
$$|A_d| = \frac{g_m R_C}{1 + g_m R_e}$$

In both cases assume a differential input and a single-ended output vC2 between the collector of Q2 and ground.
3. Design a balanced differential amplifier to meet the specifications:

- Transistors: CA3086 transistor array
- Voltage gain: Approximately 200 (single ended)
- Quiescent output voltage: 5 V
- Quiescent input voltage: Approximately ground
- AC Output Voltage: 8 V pk-pk
- Circuit Configuration: Figure 3 with Re = 0
- Make sure that the current through R1 and R2 is 1 mA or higher.

4. Calculate the expected voltage gains for the amplifier of questions 3 if IC is 1.25, and 0.75, times the design value.
5. Repeat question 4 for Re = 10, and 100 ohms.

Procedure:



CA3068

N–P–N Transistor Array

UICPS #021

1. Common Mode Gain

Note: Pin 13 of the CA 3086 is connected to the emitter of Q5 and also to the substrate. This pin must be connected to VEE whether or not Q5 is used. Arrange a circuit as shown in figure 1.

a. Check the quiescent collector voltages on Q1 and Q2.

b. Use RE = 10 kW . Use the value of VEE calculated in problem A2. Use an input signal vI = 0V by grounding the bases of Q1 and Q2. Measure VC2 and VC1. You are probably expecting values of VC1 = VC2 = 15V . Your answers will be slightly different because the resistor values for RE and RC will not be quite what you expect. Measure the resistances of RE, RC1 and RC2.

Measure the voltage across RE. Calculate the current flowing through RE. Assuming matched transistors calculate IC1, IC2, VC1, and VC2.
c. Repeat these measurements and calculations using RE = 1 kW .
d. *Common mode gain* - Using RE = 1 kW measure the common mode gain by connecting a 1 kHz sine wave to the bases of Q1 and Q2. Use an input signal with 100 mV pk-pk. Connect both the input signal and the single ended output from Q2 to an oscilloscope. Use the signal averaging feature of the oscilloscope to more precisely measure the actual pk-pk amplitudes of the input and output signals.
e. *Allowed common mode voltage range* - Connect a triangular wave voltage signal from the function generator to bases of Q1 and Q2 to measure the common mode voltage range. Connect both the common mode input and the single ended output from Q2 (or Q1) to the oscilloscope. Use a triangular wave with a peak-peak amplitude varied over the range of 1 to 5 V.

2. Differential Voltage Gain

a. Compare measured gains with the results of preliminary questions 3, and 5. An attenuator must be used to achieve a small enough input signal. To obtain balanced operation, both input ends must see the same resistance. Therefore connect the appropriate resistance to the unused input. To avoid high frequency oscillations in the circuit, shunt a 0.01 m F capacitor from the base to ground at each of the inputs of the differential amplifier.
b. Determine the value of input voltage which produces distortion in the output waveshape for each circuit (Re = 0, 10, and 100 W) when IC is at the designed value. Use VO versus VS trace to determine when distortion occurs where VS is the oscillator voltage.
c. The relation obtained in preliminary question (optional see Instructor) b2 (with Re = 0) assumes that the internal resistance between the emitter-base junction and the emitter terminal inside the transistor is zero. However, the emitter materials, the contact to the emitter, and the connecting wire of the emitter lead, all contain some resistance. Use the relation in question 2 (with Re ¹ 0) and the measured gain of procedure 1 with Re = 0 and I at its design value to calculate the net resistance between the emitter-base junction and the emitter terminal. Recalculate the expected gains of preliminary questions 4 and 5 taking into account this additional resistance and compare to the experimental results.

$$|A_d| = \frac{g_m R_C}{1 + g_m(\ r_{ee} + R_e)}$$

where ree is the emitter contact resistance.

<u>TO HAND IN ON DAY OF LAB (OPTIONAL)</u>

Do a PSpice simulation of the circuit for IC1, IC2, I as a function of

$$V_d = V_{B1} - V_{B2} \qquad \frac{V_{B1} + V_{B2}}{2} = V_{cm}$$

and

ECE - 342 EXPERIMENT V
MULTISTAGE AMPLIFIER

Purpose:
In this experiment you will combine two single stage amplifier circuits to make a multistage amplifier. Then, you will examine the gain properties of this amplifier.

Parts:
2 - 2N3053 NPN Transistors

Theory:
Practical transistor amplifiers usually consist of a number of stages connected in cascade. Such an amplifier may be desirable for a number of reasons. Additional amplification can be required to provide a signal having some specified level. We may also need to furnish a high input impedance simultaneously with a large voltage gain, or perhaps a low output impedance and a large voltage gain. The first stage can be designed for input impedance, the last for output impedance, and one or more intermediate stages for voltage gain. We may also wish to meet a large bandwidth specification by supplying a number of stages, each having low gain and large bandwidth. With any of these conditions, the solution can be obtained by designing a multistage amplifier. In this experiment a commonly used common-emitter to common-emitter to common-collector amplifier is studied from the dc and small-signal points of view.
A single common-emitter amplifier is shown in figure 1, where both source and load resistances are ac-coupled.

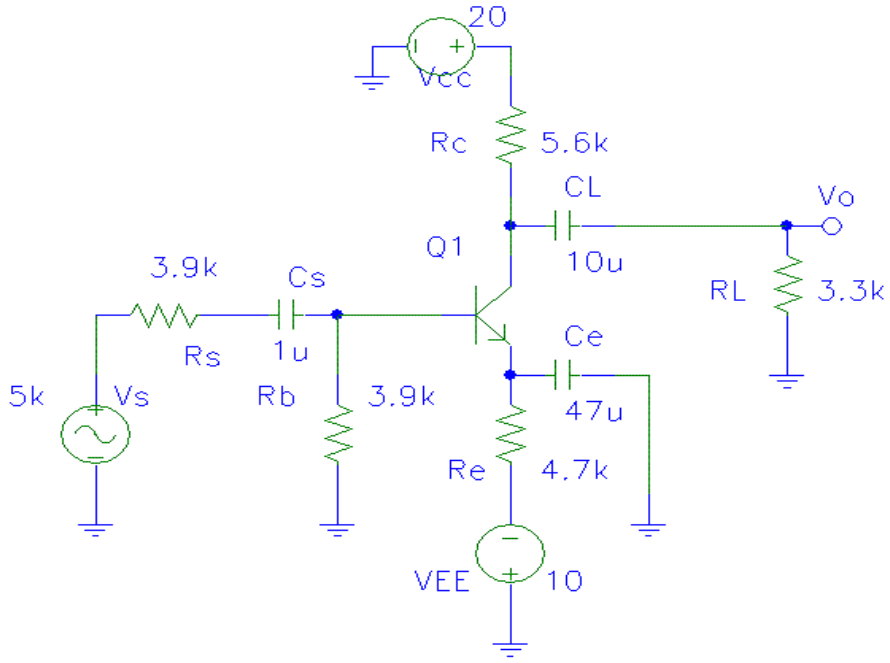


Figure 1 Common Emitter Amplifier
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Figure 2 shows the cascaded connection of common-emitter stage and common-collector stage. The circuit utilizes direct coupling between stages in order to avoid using a large coupling capacitor between stages and bias circuit.

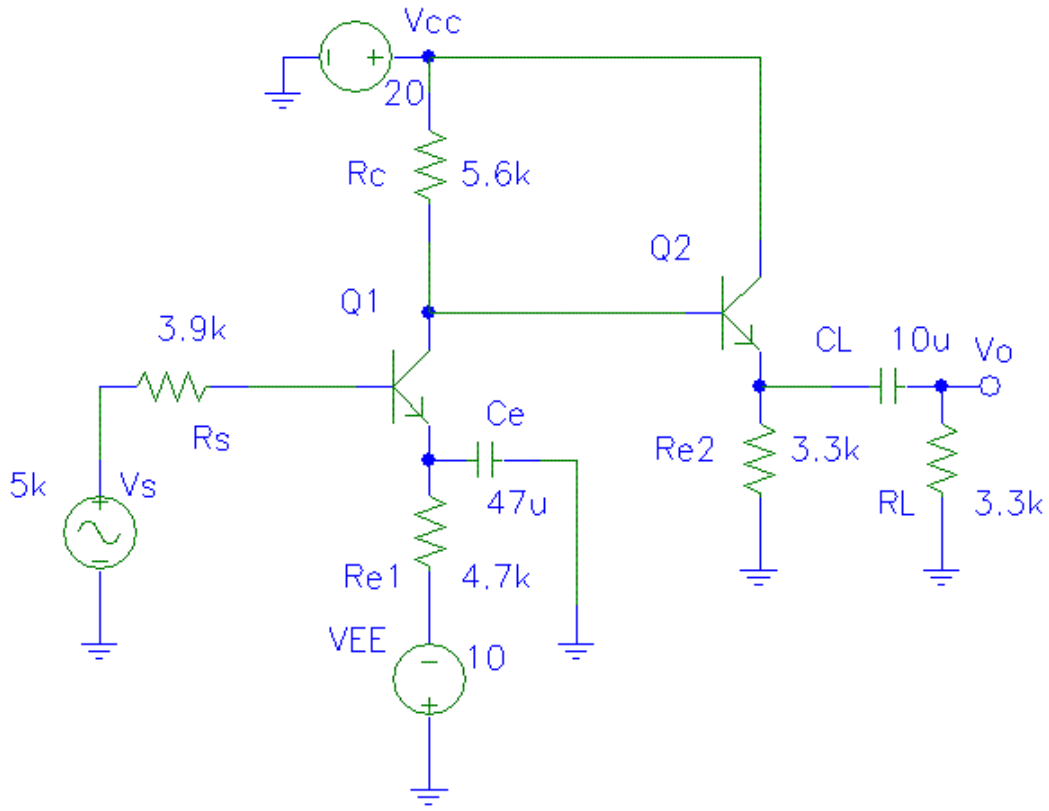

Figure 2 Common Emitter - Common Collector Amplifier

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The approximate values for the dc currents can be obtained as follows:

*I*C1 = β (VEE - Vbe) / (RS + (β+1)*Re1)

$$I_{C1} = 100\frac{10-0.7}{3.9+101\times 4.7} = 1.94\,\mathrm{mA}$$

Assuming that IB2 =0, we have

VC1 = VCC - IC1*RC = 20 – 1.94 x 5.6 = 9.14 V

VE2 = VC1 - Vbe = 9.14 – 0.7 = 8.44 V

IE2 = VE2 / Re2 8.44/3.3 = 2.56 mA

At this point a second approximation to the base current IB2 can be made:

Since IB2 << IC1, a second iteration is not necessary. The mid-frequency equivalent circuit is shown in Figure 3. Note that the emitter follower (CC stage) all components have been reflected into the base circuit.

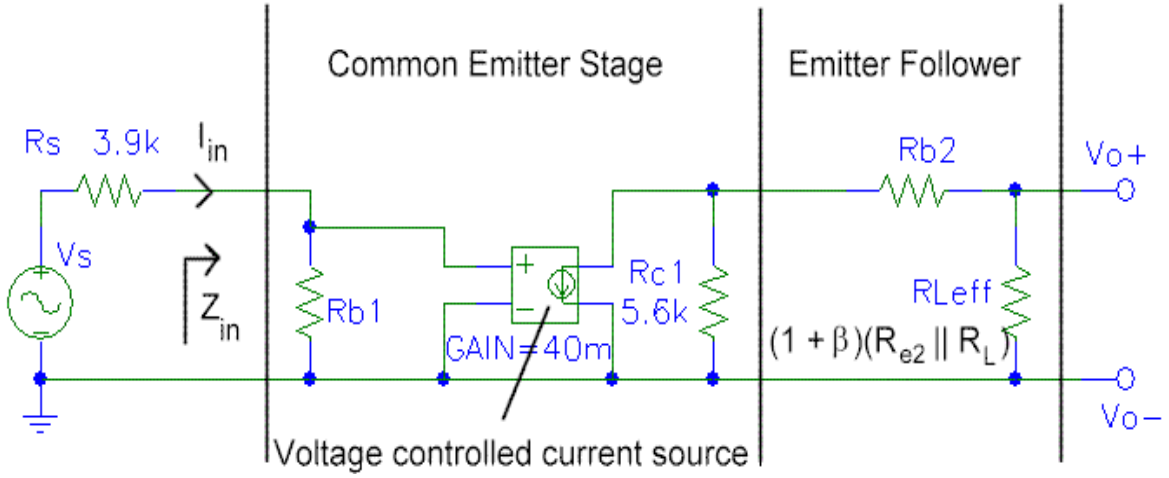


Figure 3 Small signal equivalent circuit

Procedure:

1. Construct the amplifier circuit of figure 1. Determine the Q-point conditions (measure dc values of all node voltages and branch currents).
2. Apply an input signal and determine the maximum peak-to-peak output voltage swing. What limits this?
3. Take data to plot a gain versus frequency. Determine the upper (fh) and the lower (fl) half-power frequencies or simply the cutoff frequencies (i.e., the frequencies at which the response has fallen to 3 dB below the maximum gain of the amplifier). Check the phase relationship between vs and vo.
4. Set the generator frequency to 5 kHz. Adjust vs so that the amplifier is not distorting the output signal. Measure vs and vb1 (both ac quantities) to calculate iin from the measured values by

$$i_{in} = \frac{v_s - v_{b1}}{R_s}$$

and the input impedance is then

$$Z_{in} = \frac{v_{b1}}{i_{in}} = \frac{v_{b1}\, R_s}{v_s - v_{b1}}$$

Measure the output impedance Zo using the following method:
Measure vo with, and then without the load resistance connected. The output current is calculated from:

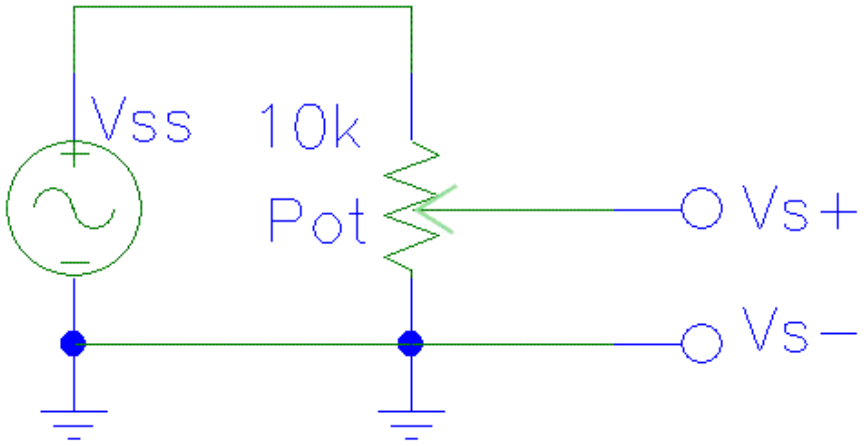
$$i_o = \frac{v_o\,|_{R_{L=33K}}}{R_L}$$

$$Z_o = \frac{\left(v_o\,|_{R_{L=\infty}} - v_o\,|_{R_{L=33k}} \right) \times R_L}{v_o\,|_{R_{L=33k}}}$$

and therefore

5. Wire the amplifier circuit of figure 2 and repeat all the procedures. Measure the voltage gain factor at 5 kHz (Determine vo/vb2 , vb2/vb1 , and vb1/vs).
6. Judging from the data obtained, explain how the emitter follower affects Zin, zo, Av, the maximum peak-to-peak output voltage swing, and the frequency response of a single stage amplifier of figure 1.

Compare the measured values for Zin, zo, Av with those determined analytically.
What causes the high-frequency gain fall-off? What causes the low-frequency gain fall-off?
When you experiment with the amplifier circuit of figure 2, modify the signal generator output as shown in figure 4.



With this circuit, a very small signal can be applied to the amplifier. The signal generator output, even when it is turned down to the minimum amplitude, would be too large for our purpose here.

ECE - 342 EXPERIMENT VI
ACTIVE FILTER DESIGN PROJECT

Purpose:
In this experiment you are asked to design a second order bandpass filter and implement it using a Delyiannis-Friend circuit.

Parts:
1 - 741 Op-Amp

Theory:
A filter is a frequency selective network. Input signals at a range of frequencies, called the pass-band, also appear at the output, perhaps only slightly attenuated. Input signals not in the pass-band, the stop-band, appear highly attenuated at the output. If two stop-bands occur on either side of a pass-band the network is called a band-pass filter. The magnitude of the transfer function for a second order band-pass filter is shown in figure 1. Two parameters serve to characterize a band-pass filter, the center frequency, w O, and the 3-dB bandwidth, BW. The Q (quality factor) of the filter is an alternative way to specify the BW. The S-domain transfer function which gives the curve shown in figure 1 is given by:

$$H(s) = \frac{Ks}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

where wo = the center angular frequency
Q = the quality factor = wo /BW
K = a constant .

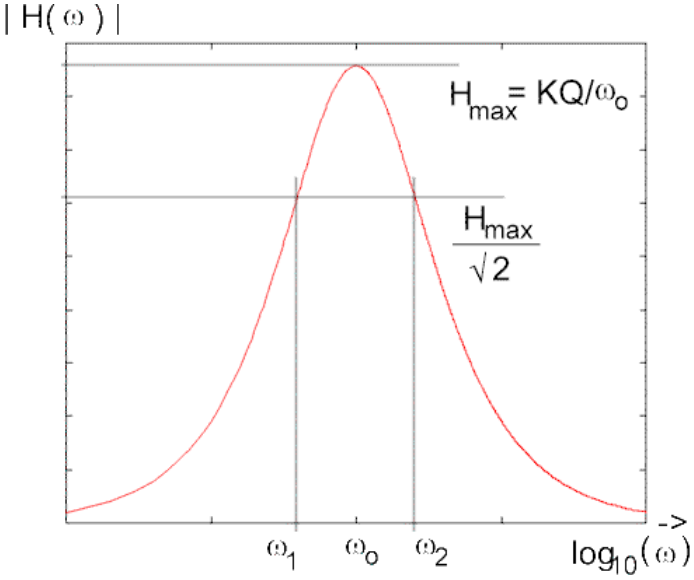


Figure 1

The curve of figure 1 is found by evaluating H(s) at s = jw and finding the magnitude of the resulting expression.

Circuits to achieve the above transfer function were originally implemented using passive elements--resistors, inductors, and capacitors. However, these circuits were cumbersome because of the bulky inductors required. However, circuits using active devices, especially op-amps, are now used to implement the above transfer function in many applications. The circuit shown in figure 2, called a Delyiannis-Friend circuit, is one of many circuits used to implement a second order bandpass filter. The transfer function for this circuit is

$$H(s) = \frac{-\left[\ 1/R_1C_1\right]\ s}{s^2 + \left[\ \left(\ 1/R_2\right)\ \left(\ 1/C_1 + 1/C_2\right)\ \right]\ s + \left[\ 1/R_1R_2C_1C_2\right]}$$

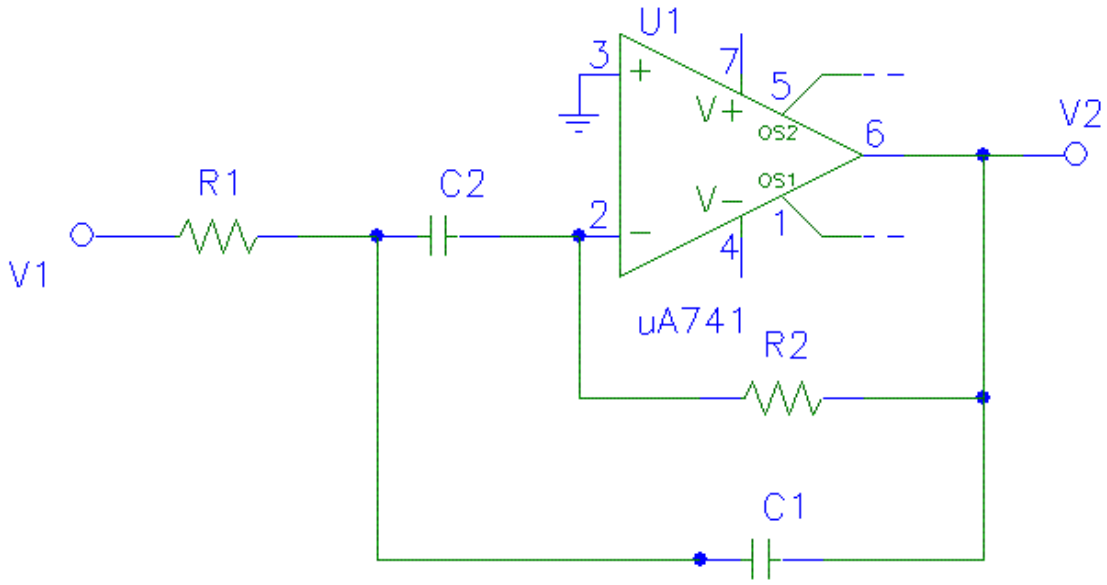


Figure 2

Procedure:

Using the circuit of figure 2, design a bandpass filter with a center frequency of 5.0 kHz and a 3-dB bandwidth of 2.0 kHz. Build and test the circuit. Compare your results with the expected filter characteristics. [Note: w = 2p f]

Questions:

Verify the transfer characteristic for the Delyiannis-Friend circuit.

ECE - 342 : EXPERIMENT VII
SINUSOIDAL OSCILLATORS

Purpose:
To investigate the conditions for oscillation, frequency of oscillation for a phase-shift and Wein bridge oscillators, and to investigate the rule of build up for the latter.

Parts:
1 - LM741 Op-Amp

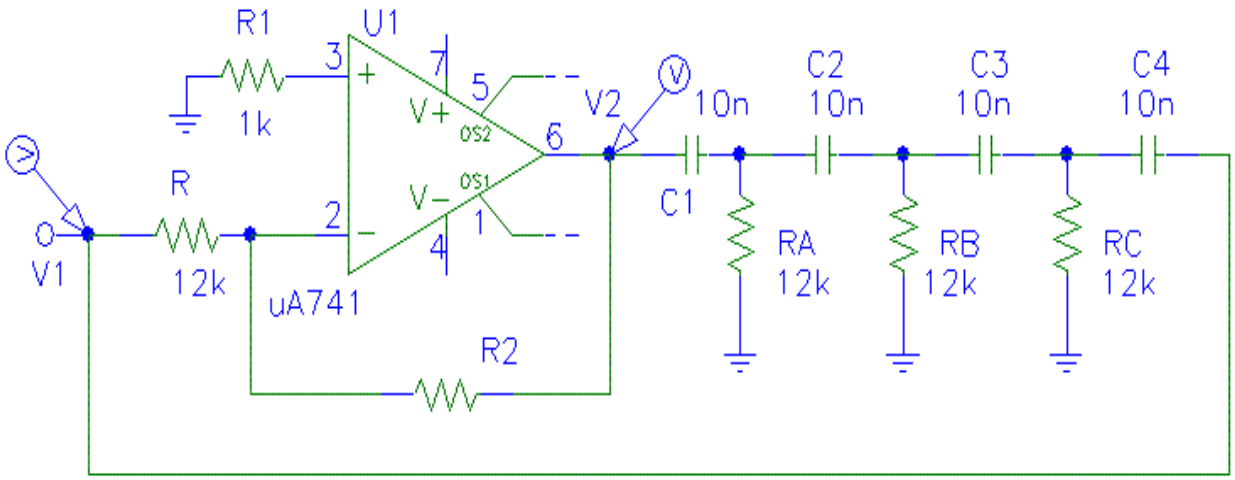


Figure 1

Theory:
1. Introduction - If a linear feedback amplifier contains reactive elements, and at some frequency the loop gain Ab = -1, sinusoidal oscillations will be obtained. The sine wave oscillators investigated in this experiment consist essentially of two separate but connected parts; the amplifier part and the frequency determining part. Probably the simplest type of feedback oscillator is shown in figure 1. Here the amplifier function is the ratio, V2 / V1 = - R2 / R and through the phase shift circuit, the ratio V1/V2 is a function of frequency. In other words the amplifier yields a phase inversion of 180° and a 180-degree phase-shift-circuit is used to produce a zero loop phase shift.

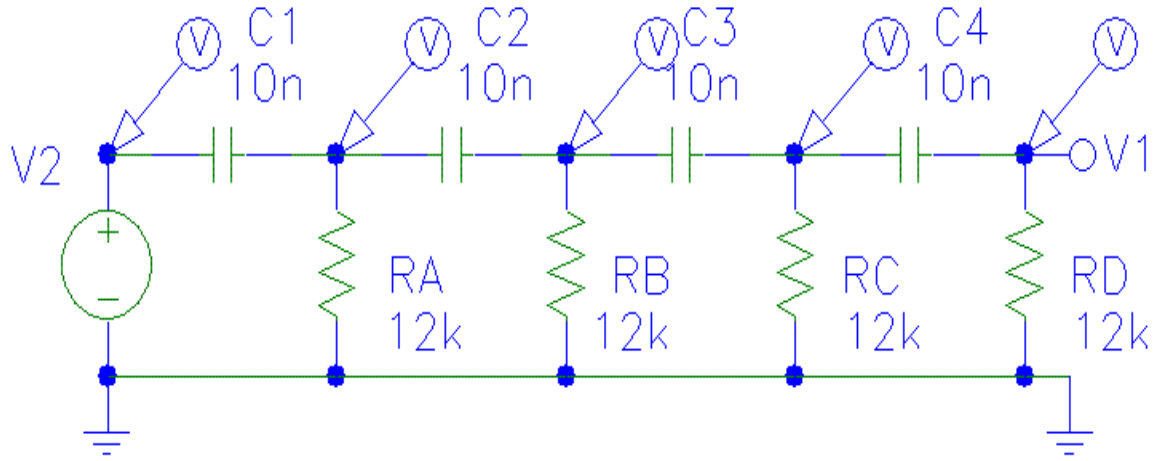


Figure 2
An analysis of the phase shift circuit, figure 2, shown that when V1 is exactly out of phase with V2

$$\frac{V_2}{V_1} = -18.4 \quad (1)$$

and occurs at a frequency of

$$\omega = \frac{\sqrt{0.7}}{CR} \quad (2)$$

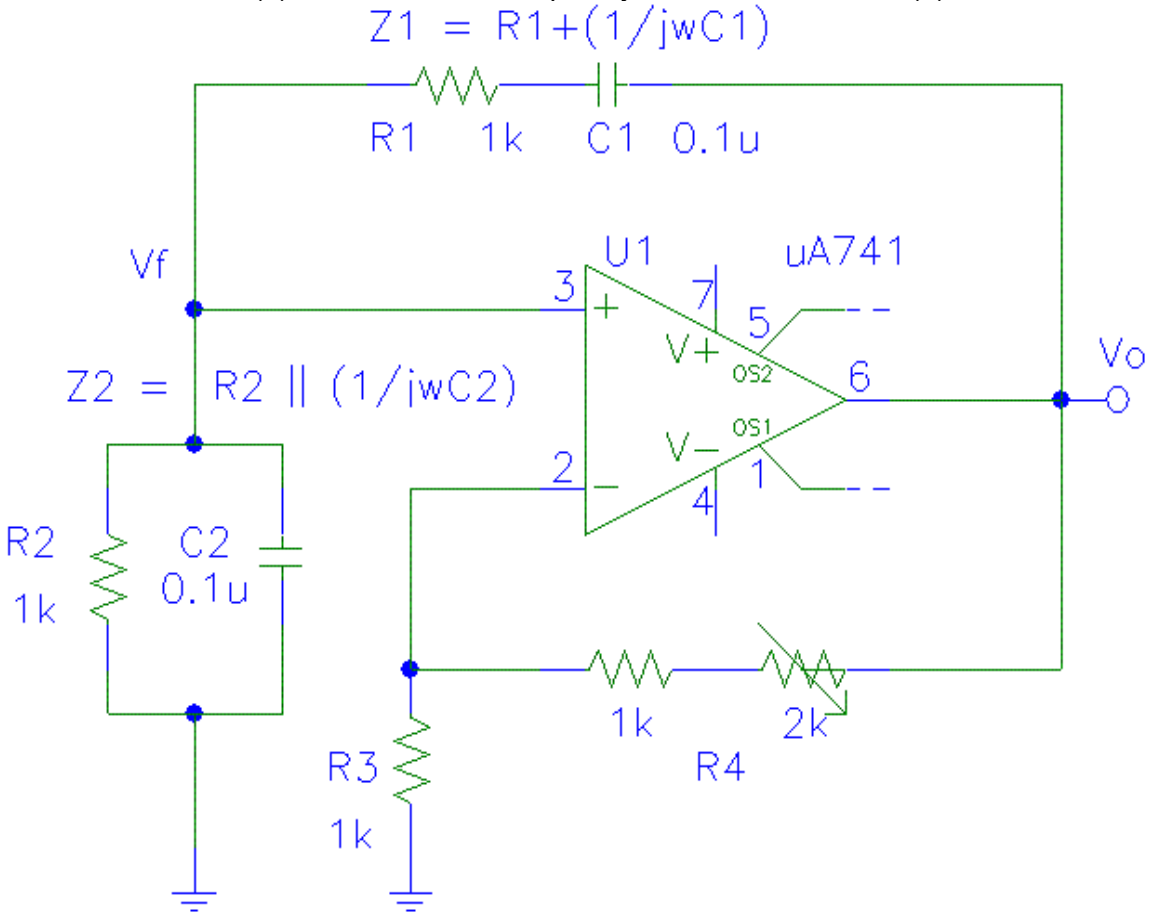


Figure 3
An oscillator circuit in which a balanced bridge is used as the feedback network is the Wien-bridge oscillator shown in figure 3. The "bridge" is clearly indicated in figure 4.

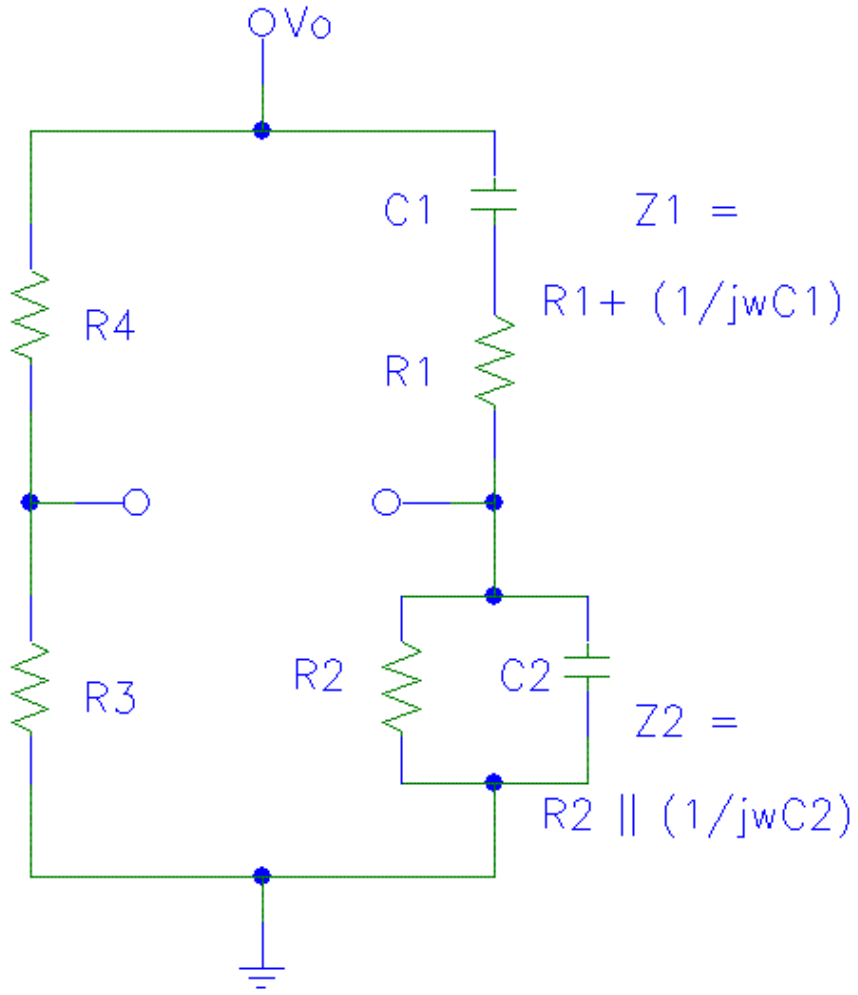


Figure 4

The four arms of the bridge are Z1, Z2, R3 and R4. The input to the bridge is the output Vo of the op. amp., and the output of the bridge between nodes 1 and 2 supplies the differential input to the op. amp. There are two feedback paths in figure 3, positive feedback through Z1 and Z2, whose components determine the frequency of oscillation, and negative feedback through R3 and R4, whose elements effects the amplitude of oscillation. The loop gain is given by -b A where:

$$\beta = \frac{-V_f}{V_o} = \frac{-Z_2}{Z_1 + Z_2} \text{ and } A = \frac{1 + R_4}{R_3} \quad (3)$$

It can be found that, with a = w RC

$$-A\beta = \frac{\alpha}{3\alpha - j(1-\alpha^2)}\left(1 + \frac{R_4}{R_3}\right) \quad (4)$$

The Barkhausen condition that Ab = -1 requires that a = 1 and

$$f = \frac{1}{2\pi RC} \text{ and } R_4 = 2R_3 \quad (5)$$

The maximum frequency of oscillation is limited by the slew rate of the amplifier. Continuous variation of frequency is accomplished by varying simultaneously the two capacitors. Changes in frequency range are accomplished by switching in different values for the two identical resistors R1 and R2.

2. Preliminary Questions

a. Verify equations (1) and (2)

b. Verify equations (3), (4), and (5)

c. Calculate the value of R4 in figure 3, which will just produce oscillation.

Procedure:

1. Phase-shift oscillator.

a. Set up the phase-shift oscillator and adjust R4 for the best output wave-form (sinusoid). Record the value of R4.

b. Observe the waveform of the signal at all nodes of the phase shift circuit.

c. Using the signal generator, determine the frequency for which the phase-shift of the phase-shift network is p radians. Record the ratio of Vin/Vout.

2. Wein-Bridge Oscillator

a. Condition For Oscillation: With an ohmmeter, adjust the potentiometer of R4 to the calculated value in preliminary question 3, and turn the circuit on. Vary the potentiometer setting and note the effect on the oscillation waveform. At what setting of R4 does the output appear most sinusoidal? What R4 just sustains oscillation. Check with an ohmmeter and compare with your calculated value.

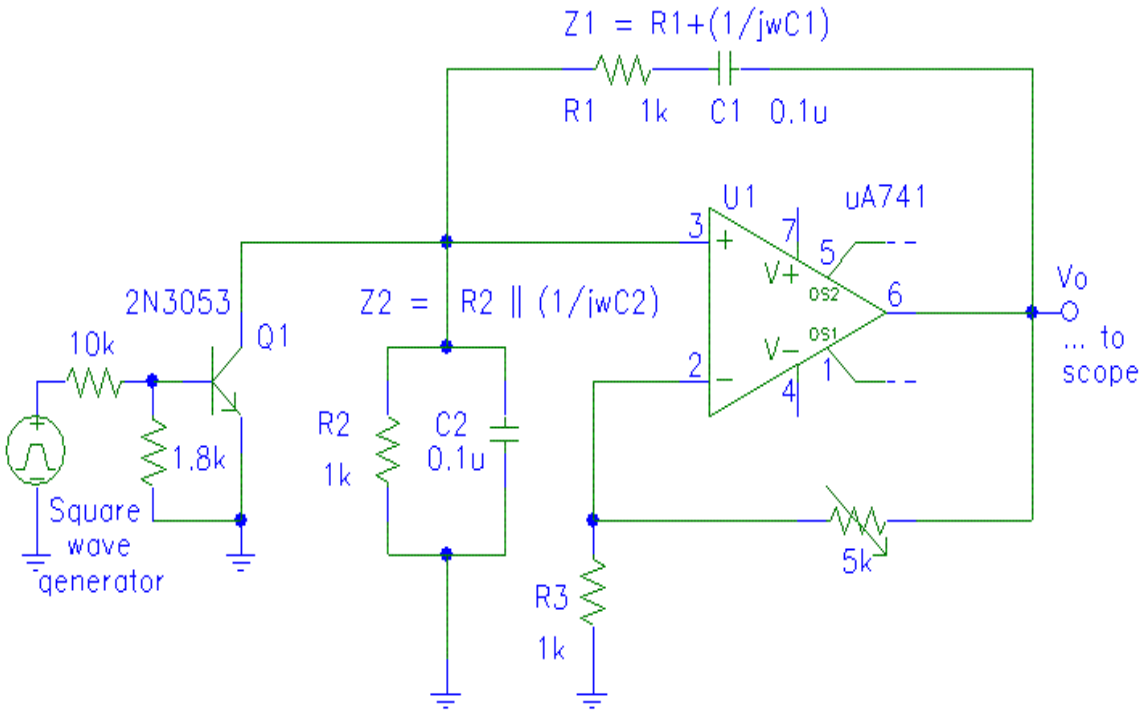


Figure 5

b. Rate Of Build Up Of Oscillation: Modify the circuit as shown in figure 5. The transistor Q1 acts as a switch and stops the oscillation when the square wave generator output is positive. When the generator output goes negative, oscillation begins to build up. The scope is also triggered

at this point. So the build up can be observed. Vary the time base until the build is visible on the screen.
What is the effect of R4 on build up rate? If a rise time is defined as the time required for the output to reach ±10 volts in magnitude, determine the rise time for R4 = 2, 2.5k, 3k, 3.5k, 4k, 4.5k, 5k, and ∞ (open circuit). Compare these values with the theoretical time constant of build up. The two values should be proportional.
c. Steady State Oscillation: Return the circuit to the original configuration; and observe the oscillator output. Vary R4 and note the effect. Open R4 and observe the waveform. What is causing the change in waveform? What is the best value of R4 in terms of distortion?

ECE - 342 EXPERIMENT VIII
WAVESHAPING AND WAVEFORM GENERATORS

Purpose:
The comparator as a basic analog building block is introduced. The regenerative comparative (Schmitt trigger) is used to generate square, triangular, and pulse waveforms.

Parts:
1 - 741 Op-Amp
2 - 1N4735 6.2V zener diode
2 - Diodes

Theory:
1. Introduction
When an op-amp is used with net positive feedback, it becomes an analog voltage comparator. If the voltage at the "+" terminal is greater (less) than the voltage at the "-" terminal, then the output voltage is at the maximum (minimum) possible value allowed by the op-amp. A comparator is used as a voltage-sensing element in threshold detectors and non-sinusoidal waveform generators.
Any op-amp may be used as a comparator. Some have been especially designed for this application. These have small offset voltages and balanced input biased currents.
2. Preliminary Questions:

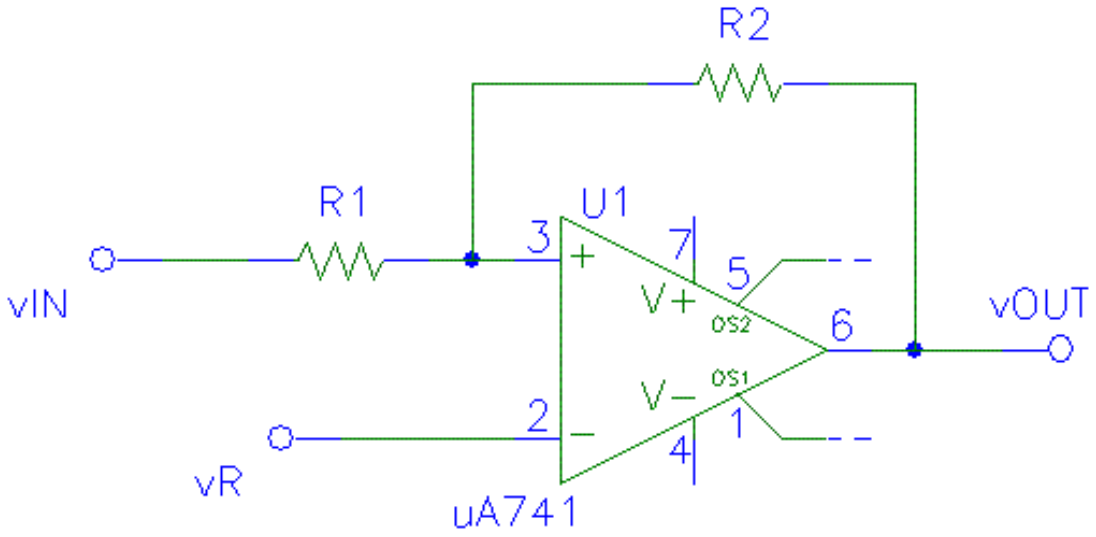


Figure 1 - Comparator Circuit
a. For the comparator circuit shown in figure 1,
(1) Find expressions for the threshold voltages VT1 and VT2 in terms of R1, R2 and op amp limited voltage (of magnitude VO). Explain your calculations.
(2) Plot the transfer characteristic and display the direction of switching levels.
(3) If VR = 0, VT2 = -VT1 and an input sinusoid of frequency, f = 1/T , is applied to such a comparator, the output will be symmetrical square wave, of half period T/2. The vertical edge of the output waveform will not occur at the time the sine wave passes through zero, but will be shifted in phase by q, where sinq = VT2 / Vm and Vm is the peak sinusoidal voltage. Plot this statement by drawing clearly the output lined up in time with the input, showing delay time if a 4V peak sinusoid is applied and R2 = 5R1. Assume the peak output is 14V.

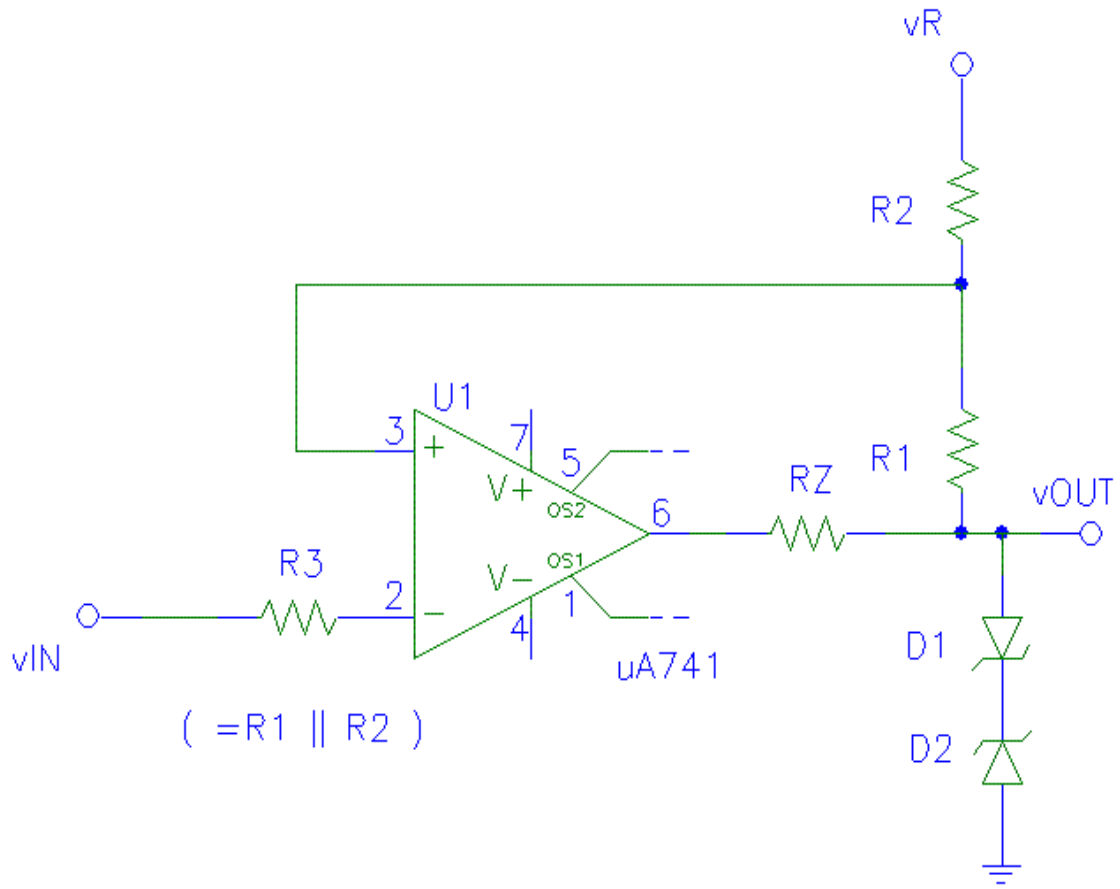


Figure 2 - Inverting Schmitt Trigger

b. An op amp with an open loop gain AV of 14,000 is used to construct the circuit in figure 2. The threshold levels desired are 3± 0.2V .

(1) Find the ratio R2/R1. What physical conditions determine the choice of the individual resistances?

(2) Find the loop again. Does it satisfy the requirement for regenerative switching?

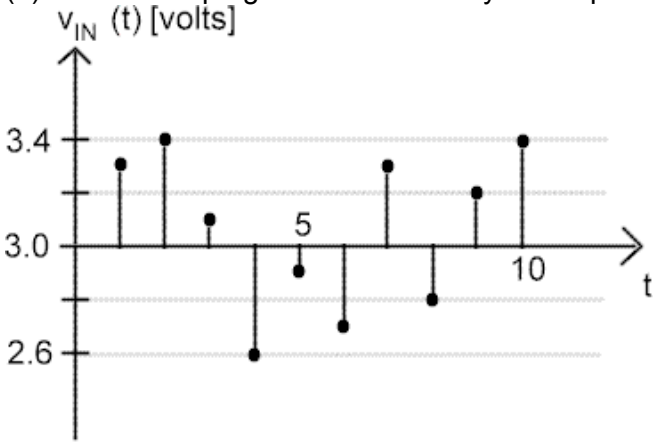


Figure 3

(3) If the input Vi(t) to the Schmitt trigger is the set of pulses shown in figure 3, plot the transfer characteristic of the Schmitt trigger. Plot the output waveform VO(t) lined up in time with Vi(t).

(4) Find VR.

(5) Is it possible to set the threshold voltage at a negative value? If no, explain why not? If yes,

how? How must VR be chosen so that VT1 is negative, but not VT2?
(6) How must VR be chosen if VT1 = -VT2? With your newly chosen VR and from preliminary question a(3), draw clearly the output lined up in time with the given sinusoid input if R1 = 13R2. Show all relevant values.
(7) If the threshold voltage VT2 is zero and the hysteresis is VH = 0.2V. Calculate the time duration of the positive and negative portions of the output waveform for a 1KHz sine wave input whose peak-to-peak value is 4V. Draw the output waveform lined up in time with the input and show all relevant values.
(8) For the Schmitt trigger circuits, as the loop gain | b Av | increases from zero to unity we note that the transfer gain Avf increases from 14,000 toward infinity. There is no hysteresis as long as -b Av ≈ 1. Elaborate on the consequences resulting from an adjustment which ensures that the maximum loop gain is unity (b Av = 1). Avf = Av / (1 - b Av)
(9) In practice, a loop gain in excess of unity is chosen and a small amount of hysteresis is tolerated for the Schmitt Trigger explain what will happen if the threshold voltage range is larger than the peak-to-peak signal.
(10) If noise spikes, positive and negative are present on the input signal to the circuits in the neighborhood of the amplitude VR. Explain why the output may "chatter" (i.e., change from one state to the other). Is this difficulty avoided in a Schmitt trigger (i.e., when positive feedback or regeneration is added to a comparator)? Explain.
(11) Sketch the circuit of a noninverting Schmitt trigger. Find expressions for the threshold levels VT1 and VT2. Plot the transfer characteristics and show all relevant values. Draw the output waveform lined up with time with a sinusoid input signal.
c. Square Wave Generator.

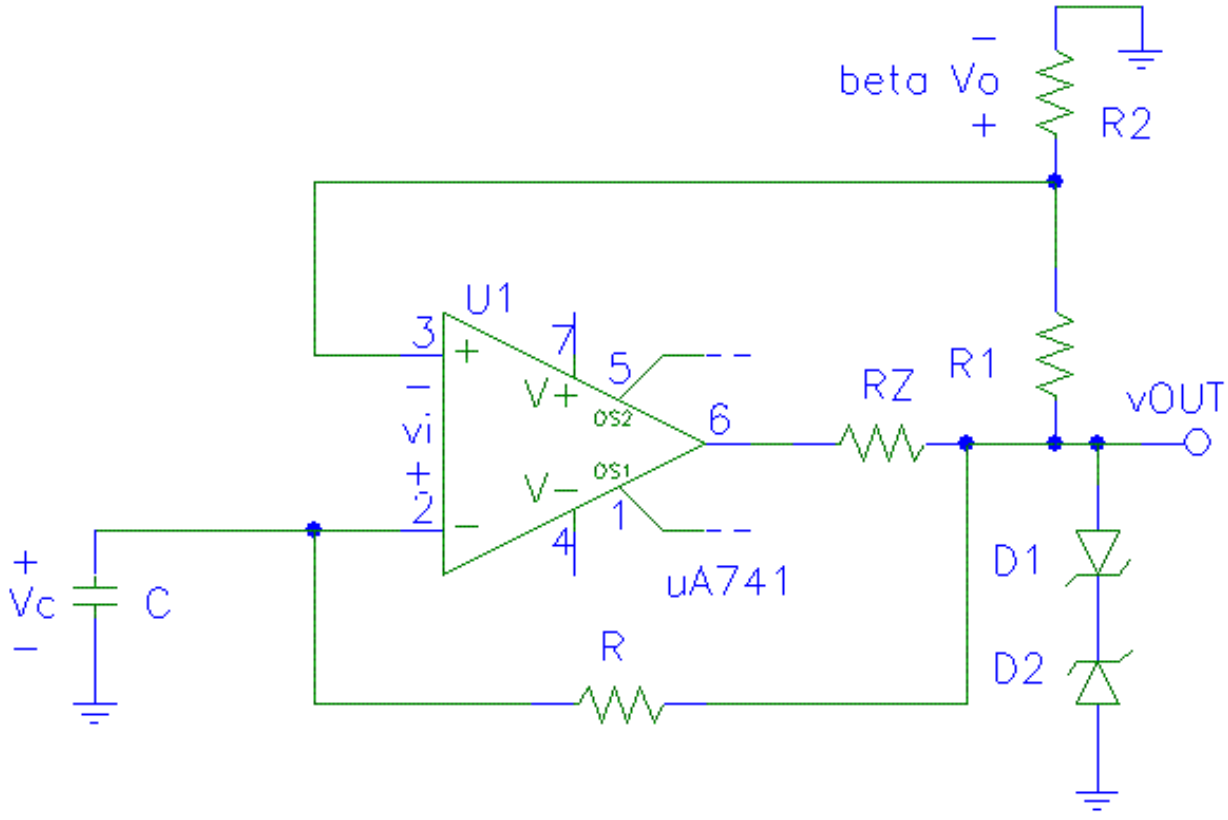


Figure 4 - Square wave generator
(1) Find appropriate values for the resistive and capacitive components of the square-wave

generator in figure 4 to give 1msec period of oscillation. Let the feedback factor = 0.5, R = 100 kW, and RZ = 1 kW. RZ is used at the output of the op-amp to limit the output current drawn when the zener diodes conduct. It need not be included in any analysis equations.
(2) Plot the output and capacitor voltage waveform, and show all relevant values.
d. Triangular Wave Generator

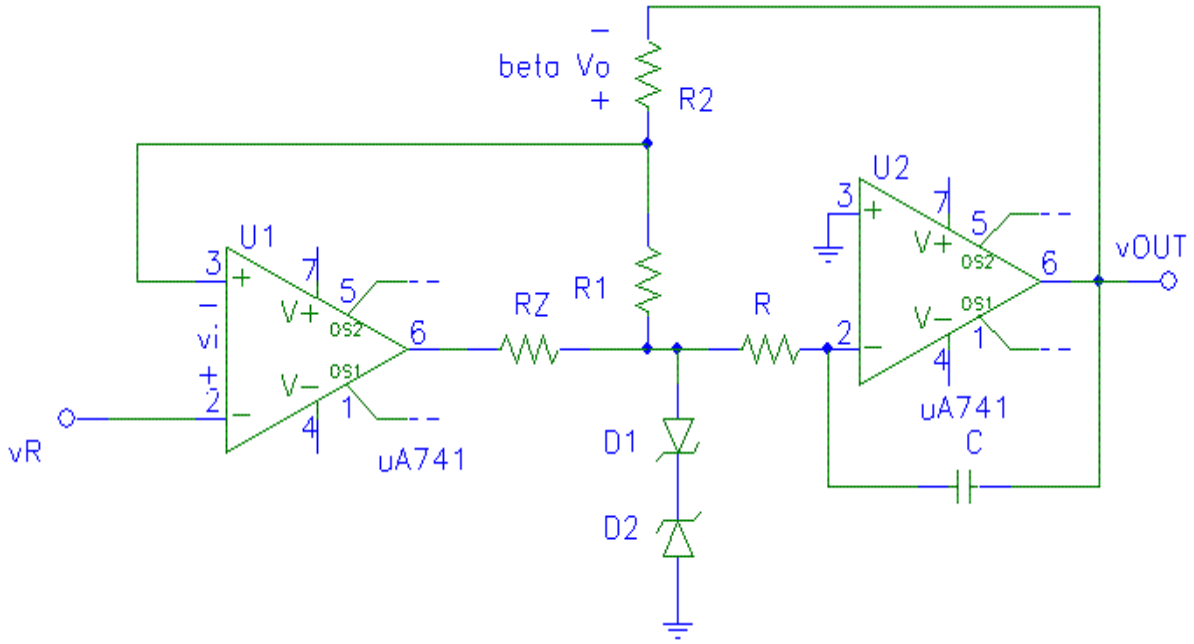


Figure 5 - Triangular wave generator
For the triangular-wave generator is figure 5, given that: RZ = 10 kW, R2 = 8.2 kW, C = 0.1 ⁄F and the following series combination, R1 = 10 kW + 10 MW pot. , R = 1.5 kW + 150 kW pot. Calculate and then plot the output v(t) with all relevant values Vmax, Vmin, Rise Time, Fall Time, etc) when vR = (i) 0 V, (ii) 1 V. Assume all potentiometers are set at the center.
e. Pulse Generator
A monostable multivibrator has one stable state and one quasistable state. The circuit remains in its stable state until a triggering signal causes a transition to the quasistable state. Then after a time T, the circuit returns to its stable state. Hence a single pulse has been generated, and the circuit is referred to as a one-shot or single-shot.
To see how the circuit operates, assume that it is in its stable state with the output at vO = +VO and the capacitor clamped at the diode D1 on voltage VD ⁄0.7 V (with b VO > VD). If the trigger amplitude is greater than b VO - VD, it will cause the comparator to switch to an output vO = v-VO. As indicated in figure 7, the capacitor will now charge exponentially with a time constant t = RC through R toward -VO because D1 becomes reverse-biased. When vCbecomes more negative than - b VO, the comparator output swings back to +VO. The capacitor now starts charging toward +VO through R until vC reaches VD and C becomes clamped again at vC = VD.
To find the pulse width T. When the triggering pulse occurs, the capacitor C starts charging from an initial value VD towards a final value -VO, therefore

$$v_c(t) = -V_o + (V_D + V_o)\, e^{-t/RC} \quad (1)$$

At t = T, $v_c(t) = -V_o = -V_o + (V_D + V_o)\, e^{-T/RC}$ (2)

and solving for T we obtain,

$$T = RC \ln \frac{1 + V_D / V_o}{1 - \beta} \quad (3)$$

If VO >> VD and R2 = R1 so that b = 1/2, then T = 0.69 RC.
The triggering pulse width TP must be much smaller than the duration T of the generated pulse. For short pulse width T the switching times of the comparator become important and limits the operation of the circuit. The diode D2 is not essential but it serves to avoid malfunctioning if any positive noise spikes are present in the triggering line. If RZ = 0 and the Zener diodes are omitted. Equation (2) remains valid with VO = VCC – VCE,sat.
Note that the capacitor voltage vc does not reach its quiescent value vC = v1 until time T' > T. Hence, there is a "recovery time" T' - T during which the circuit may not be triggered again and so the next synchronizing trigger must be delayed from the previous input pulse by at least T$_{\text{R}}$ seconds.

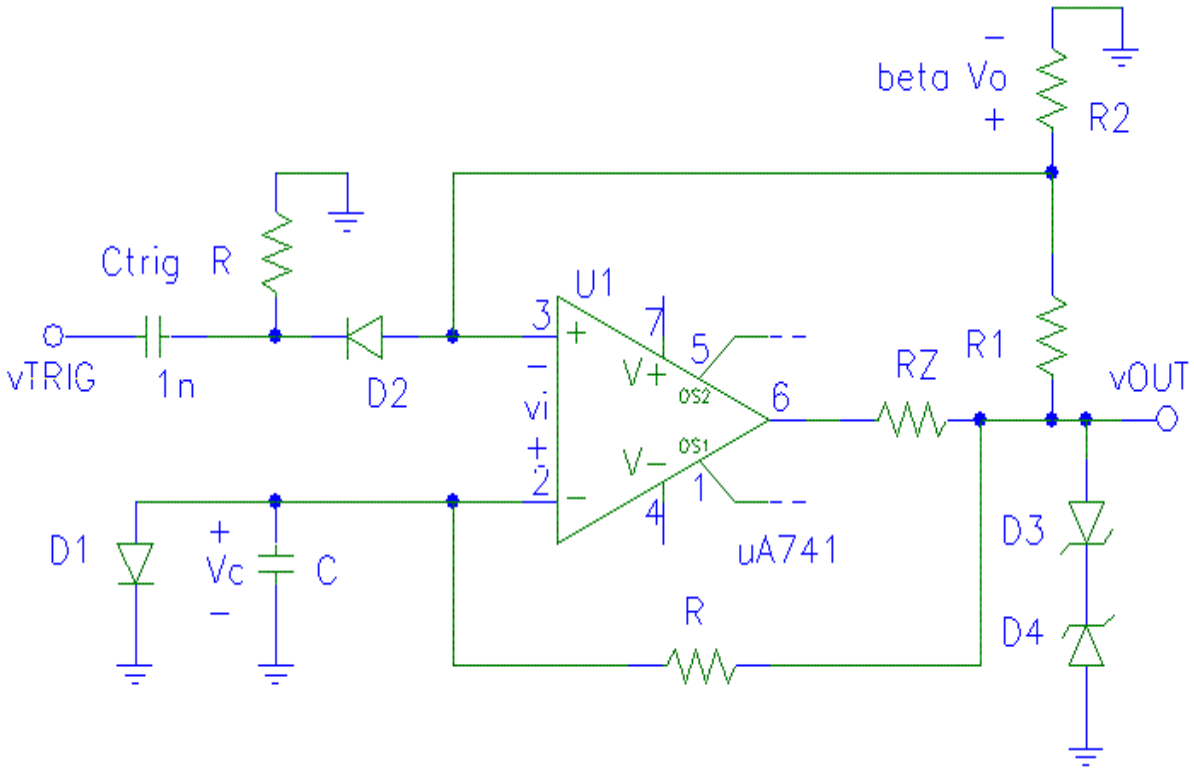


Figure 6
(1) Find appropriate values for the resistive and capacitive components of the pulse generator in figure 6 to give 1 msec pulse output. Let the feedback factor b = 0.5, RZ = 10 kW. Assume that VO $_{\text{R}}$ VD .

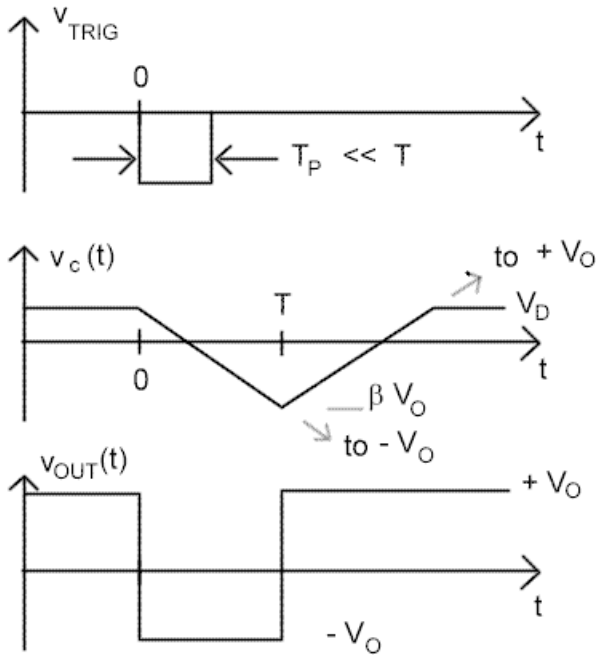


Figure 7

(2) Calculate all values shown in figure 7 and plot the output and capacitor voltage waveforms.

Procedure:

1. Construct an inverting Schmitt trigger of the form shown in figure 2. Let RZ = 10 kW, R1 = 10 kW, R2 = 100 W, and VR = (a) 0 V, (b) 1V. Plot input and output superimposed and its transfer characteristics. How do the calculated values compare with experimental results? Repeat the procedure above for a noninverting Schmitt trigger.
2. Construct the circuit in preliminary question 3. Verify its operation. Plot and record all results. Compare with the theoretical results.
3. Repeat question 2 above for preliminary question 4. Explain your observations for the two values of VR.
4. Repeat question 2 above for preliminary question 5.

ECE - 342 EXPERIMENT IX
CMOS APPLICATIONS

Purpose:
In this experiment, you will examine the ways to interface the TTL family and the CMOS logic family of digital integrated circuits. Also, you will design and build an astable multivibrator using CMOS NAND gates.

Parts:
1 - 4011 Quad 2-input CMOS NAND gate
1 - 7400 Quad 2-input TTL NAND gate
2 - 2N3053 NPN transistor
CMOS Transmission gate

Theory:
1. TTL-to-CMOS Interface
When used with a 5-V power supply, CMOS is somewhat compatible with TTL. In the Low state, a TTL output can drive CMOS directly. However, the guaranteed TTL HIGH output level of 2.4 V is not a valid input level for CMOS. If a TTL output drives only CMOS, then there is essentially no output current and the HIGH output level may be 3.5 V or higher. Whether this is sufficient for a reliable interface depends on the exact manufacturer's specifications for both the TTL outputs and the CMOS inputs. A valid HIGH output level can always be ensured by typing a pull-up resistor from the TTL output to the 5 V supply.
2. CMOS-to-TTL Interface
When CMOS drives TTL the HIGH state is not a problem. The crucial question is whether CMOS can sink TTL input current in the LOW state without exceeding the maximum value of the TTL LOW-state input voltage. The reason for this is that when the input of a TTL gate is LOW, the input transistor is conducting in the forward direction. Therefore a current is flowing out of one of the emitters of the input transistor, and this current must flow into the circuit connected to the TTL input. Typical CMOS gates are specified to sink about 0.4 mA in the LOW state while maintaining an output voltage of 0.4 volts or less. This is sufficient to drive two low-power TTL inputs or one low-power Schottky input, but it is insufficient to drive standard TTL. Close examination of the specifications may show that it is possible to drive standard TTL at room temperature with some loss of DC noise margin. However, it is better to use a special buffer such as a 4041 to drive standard TTL from CMOS.
3. CMOS Transmission Gate
The CMOS transmission gate circuit and circuit symbols are indicated in figure 3. The transmission gate transfers the input signal to the output, if and only if C is HIGH and is LOW. These transmission gates are made using MOSFETs with positive threshold voltages. When the input is HIGH then the source-to-gate voltage of the PMOS transistor is a large enough to turn on the PMOSFET. This creates a conducting channel between the input and output terminals. If the input signal is LOW then the gate-to-source voltage of the NMOS transistor is large enough to turn the NMOSFET on, again creating a conducting channel between input and output. If C is LOW and HIGH then both MOSFETs are off no matter what the input signal is.

Procedures:

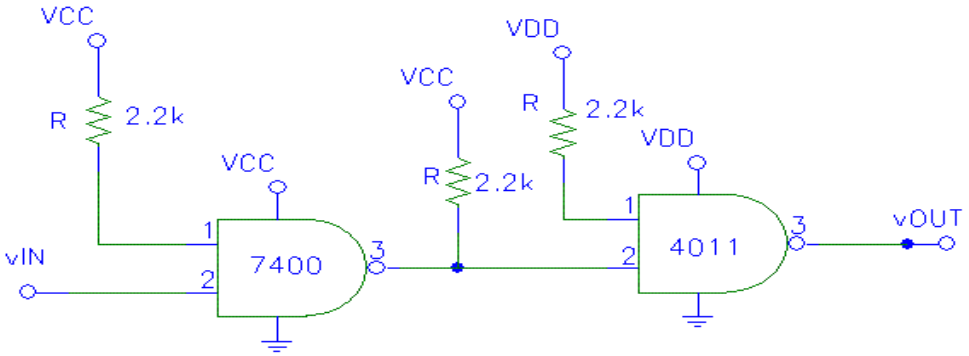


Figure 1a

VCC = VDD = 5 volts

R = 2.2 k ohms

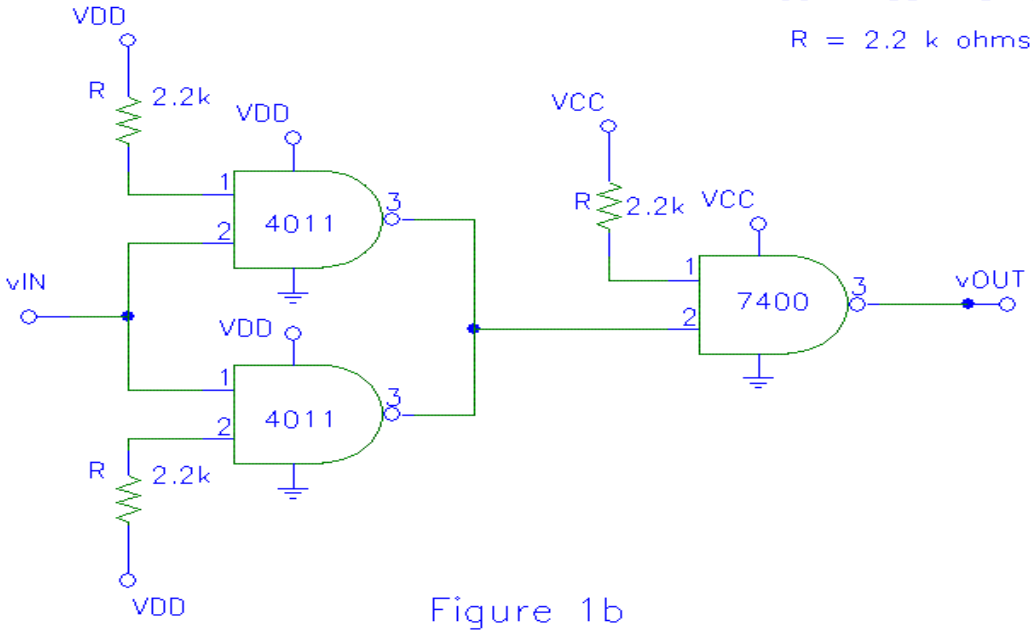
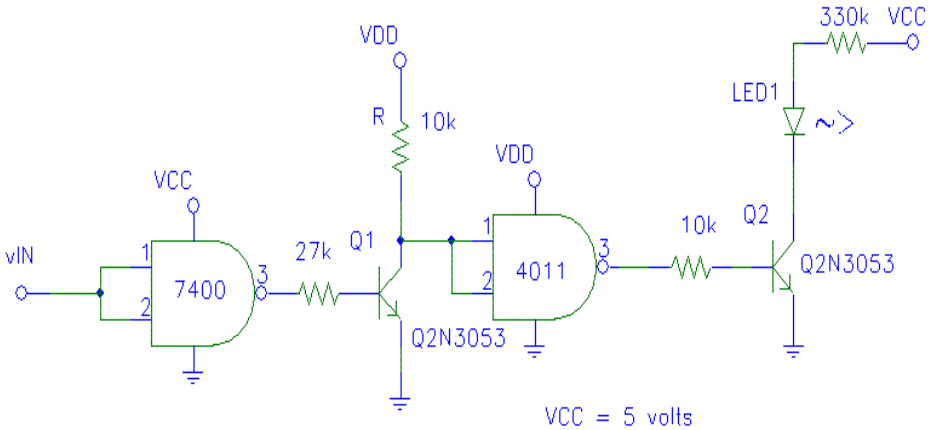


Figure 1b

1. TTL/CMOS interface

a Simple interfacing Build the circuits shown in figure 1. Measure the propagation delay from input to output of a TTL pulse.



VCC = 5 volts

VDD = 3 to 15 volts

Figure 2

b. TTL/CMOS interface using an npn transistor. Wire the circuit as shown in figure 2. Adjust the frequency of the clock so that the LED monitor flashes approximately once each second. The npn transistor is used to overcome the incompatible logic levels that exist between the TTL driver and the CMOS load. When used, the transistor stage inverts the input signal so that when the input to the transistor stage is at (TTL) logic 1, the collector voltage is essential at 0 volts since the transistor is driven into saturation. When the input is zero (TTL-logic 0), the collector voltage is nearly that of the CMOS supply, since the transistor is cut off. Increase the supply voltage VDDfrom 3 volts to 15 volts. Is there any difference in the operation of the circuit?

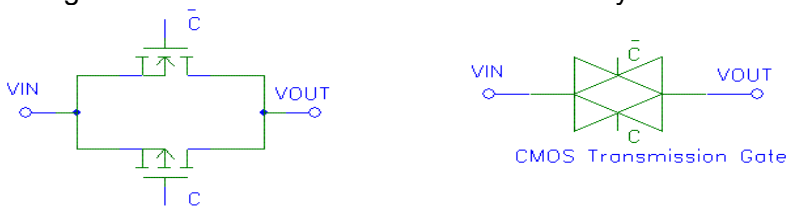


Figure 3

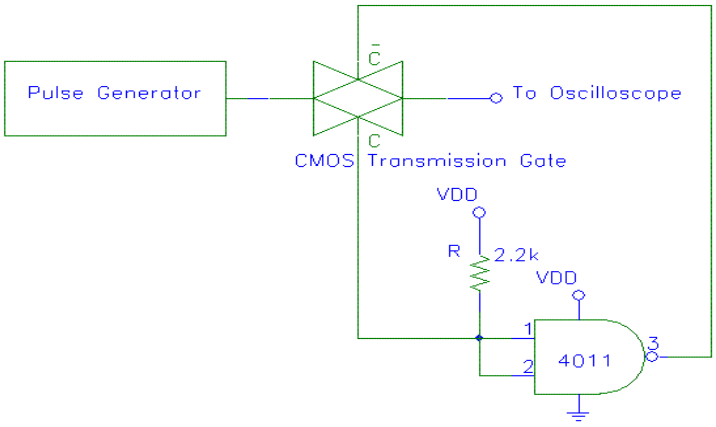


Figure 4

2. CMOS Transmission Gate

Set up the circuit of figure 4. Sketch the input and output waveforms. Measure the propagation delay of the CMOS transmission gate. Now set C LOW (0 V) and C HIGH (5.0 V). What output signal do you see?

(Hint: Use the QUAD analog switch in your kit)

ECE - 342 EXPERIMENT X
TTL LOGIC GATES

Purpose:
This experiment is intended to demonstrate the electrical characteristics of the basic TTL-gate.

Parts:
1 - 7400 or 74500 or 74L500 QUAD 2-input NAND gate.

Theory:
1. Basic TTL Gate

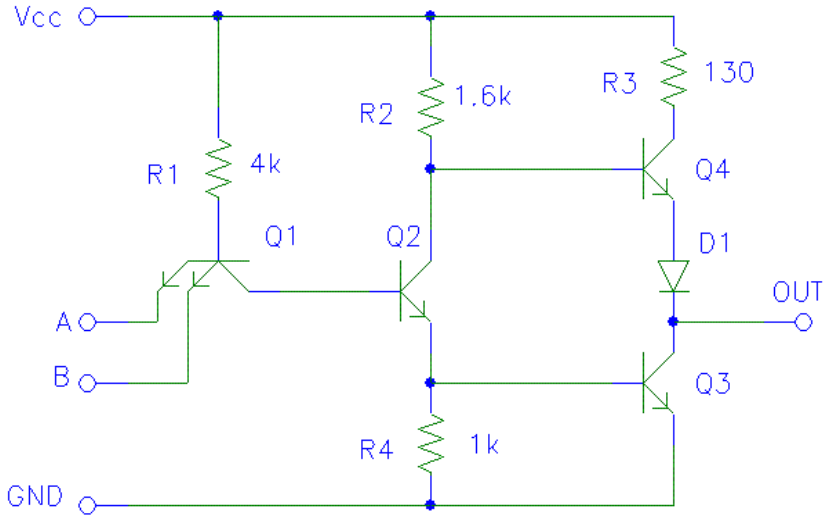


Figure 1
The basic two-input TTL NAND-gate (1/4 of a 7400) is shown in figure 1. The characteristic will be slightly different for 74S00 or 74LS00. The power supply Vcc is +5 volts. When all inputs are HIGH (> 2 volts) the current in R1 flows through the collector of Q1 into the base of Q2, turning on Q2. This turns on Q4 and turns off Q3, and the output voltage is LOW. If any input goes LOW (< 0.8 volts), the current in R1 flows through emitter of Q1, out of the input lead into ground. Q2 is turned off, turning off Q4 and turning on Q3, resulting in a HIGH output voltage. Except during the transitions, transistors Q1, Q2 and Q4 are always either saturated or cut off. The output structure consisting of Q3 and Q4 is called *totem pole*. A Darlington pair to increase the HIGH output drive capability sometimes replaces Q3 in this structure.

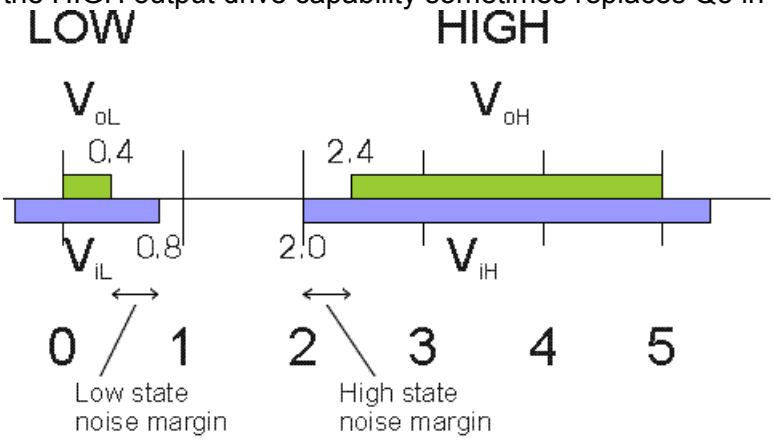


Figure 2 - TTL Logic Levels
2. Logic Levels, Noise Margins, and Fan-out
The voltages corresponding to logic levels of standard TTL are depicted in figure 2. VOL is

the guaranteed maximum output voltage in the LOW state, 0.4 V for standard TTL. VoH, the guaranteed minimum output voltage in the HIGH state, is 2.4 V. VIL is the maximum input voltage guaranteed to be recognized as a LOW. Since VIL is 0.8 V, it exceeds VOL by 0.4 V, and there is a DC *noise margin* of 0.4 V in the LOW state. VIH, the minimum input voltage guaranteed to be recognized as a HIGH, is 2.0 V. Thus, there is a DC noise margin of 0.4 V in the HIGH state also.

All the parameters above are guaranteed by the manufacturers of TTL over a specified range of temperature, power supply voltage, and fanout. The maximum fanout of standard TTL is 10, as we shall see below.

In the LOW state, a standard TTL input requires 1.6 mA of sink current (guaranteed maximum). A standard TTL output is guaranteed to sink at least 16 mA of current in the LOW state. The 1.6 mA is sometimes referred to as a *LOW-state unit load*.

In the HIGH state, a standard TTL input requires a sources of 40 mA of current (guaranteed minimum). A standard TTL output is guaranteed to source at least 400 μA of current in the HIGH state. Hence one standard TTL output can drive 10 standard TTL inputs in the HIGH state. The 40 μA is sometimes referred to as *HIGH-state unit load*.

TTL gates with Darlington pairs in the totem pole output have more driving capability in the HIGH state. They can typically source 800 μA and hence they have a fan-out of 20 in the HIGH state only. What good is increased fan-out in only the HIGH state? The answer is as follows. When two inputs of the same gate are tied together, as in a two-input NAND gate used as an inverter, the LOW-state input current is only 1.6 mA and the two tied inputs look like only one LOW-state unit load. However, in the HIGH state, the tied inputs look like two unit loads. Hence, the increased HIGH-state fan-out capability allows gate inputs to be tied together without reducing the total number of gates that can be driven.

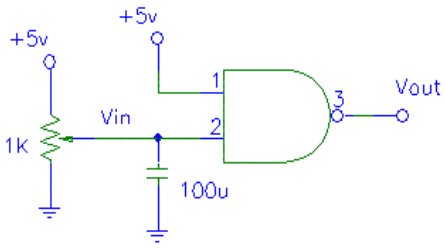
Other TTL families have different output voltage levels and input and output currents. These are described in the subsequent section. When dealing with a single family it is usual to define unit loads to facilitate fan-out calculations. However, when different families are interconnected it is necessary to sum the individual input currents and compare with the output drive capability to check that fan-out capabilities have been exceeded.

The effect of loading an output with more than its rated fan-out is to increase its LOW-state output voltage and decrease its HIGH-state output voltage. Because of TTL's DC noise margins, a slightly overloaded circuit will still work in noise-free conditions, but of course the noise margins are reduced.

Unused inputs of TTL gates, left floating, behave as if they have a logic 1, applied to them, but a small amount of noise can change this to a 0. Therefore, unused TTL inputs should be tied to a source of logic 1. Tying directly to the 5 V supply is not recommended since a transient over 5.5 V as short as a few nanoseconds can damage the gate. Instead, tie unused inputs to a 5 V supply through a current limiting resistor (1kΩ is good enough for 50 inputs), or use the output of an unused NAND gate with one of its inputs grounded.

Procedure:

1. For each of the following three experiments, you are to set up the indicated circuit and plot the variable values choosing appropriate scales that display there gross behavior. Use the same TTL NAND gate (1/4 of a 7400) for all three experiments.



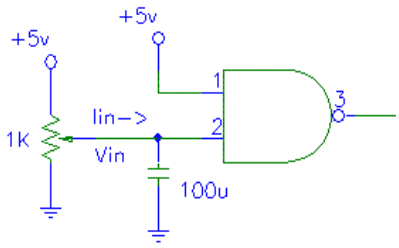


Figure 3 Figure 4

a. Measure the output voltage versus input voltage: see figure 3.

b. Measure the input current versus input voltage: see figure 4.

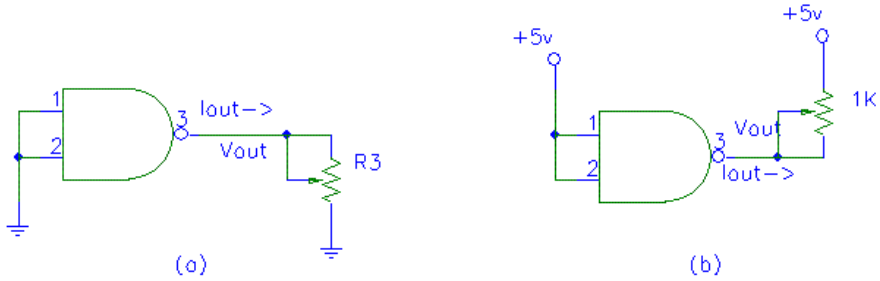


Figure 5

c. Measure the output current versus output voltage: see figure 5.

1) Zero-state

NOTE: In this part, do not let output current exceed 10 mA for more than one minute, otherwise, the gate will be damaged.

2) One-state

d. Some questions for your report:

1) What would be the output voltage for a gate with no connections to the input (Iin = 0 amps)? Would it be wise to use no-connection as a constant logic-value? Explain.

2) Using your results, calculate the maximum fan-out for an output in the low state. You should assume a DC noise margin of 0.4 V.

3) Again, assuming a DC noise of 0.4 V, what would be the maximum fan-out or an output in the high state?

4) Why do you think the manufacturer of the chip specifies 10 as the maximum fan-out?

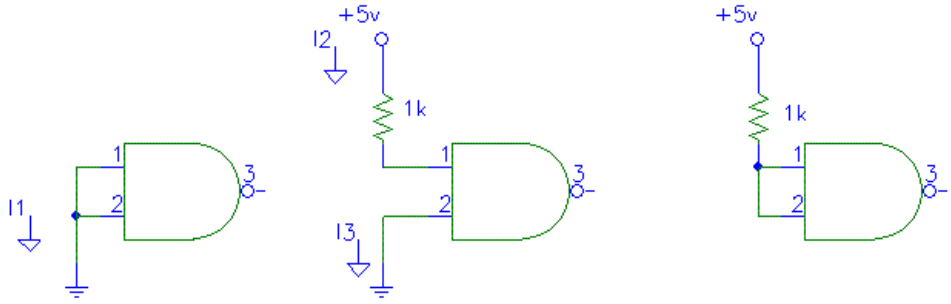


Figure 6

2. Measure the following four currents (as indicated in the figure 6):

What does this imply about fan-out when several inputs of one gate are tied together?

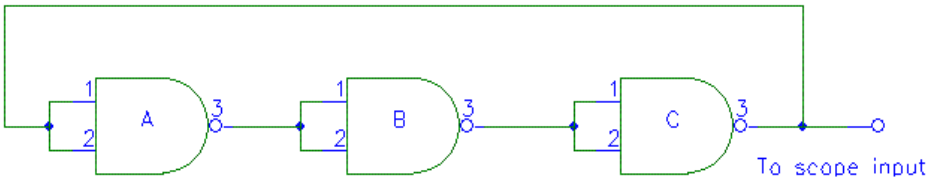


Figure 7

3. Propagation delay time

Any odd number of inverters will oscillate if they are tied together in a ring as shown in figure 7 (this is called a Ring Oscillator). This circuit confuses some people because they are accustomed to seeing sinewave oscillators implemented with positive feedback, or amplifiers with non-inverting gain. Since the concept of phase shift is a little strained when the inverters remain in their linear region for such a short period, it is far more straightforward to analyze the circuit from the standpoint of ideal switches, with a finite propagation delay, rather than as amplifiers with 180 degree phase shift. It then becomes obvious that a '1' chases itself around the ring, and the circuit oscillates. The frequency of oscillation will be determined by the total propagation delay through the ring and is given by the relation:

$$f = \frac{1}{2Nt_{pd}}$$

f = frequency of oscillation.
tpd = propagation delay per gate.
N = number of gates.

a) Display the waveform for the ring oscillator. Observe the period of oscillation and calculate the average propagation delay time, using the above relation.

b) Calculate the speed-power product for the TTL gate prsp. delay (n s) x (m w) = p J = speed power product for (1) static case and (2) dynamic use and compare.

c) Connect a 50 pF capacitor at each node of the ring oscillator circuit (This approximates a loading of about 10 similar gates). Observe the waveform and explain the effect of fanout (the load gates) on the parameter tpd.

Report Suggestions:

Answer the questions, plot the observed waveforms, and record the measurements of the procedure section.