CS/ECE 252
Exam 4 Review
11AM section
2015 December 11
Before we get started

Homework 8 due at beginning of lecture

Exam 4 on Monday, December 14th, during class

Today: Exam 4 Review

(Extra) office hours for HW8 and Exam4: see Piazza

Quote of the day:
“Inspiration exists, but it has to find you working”
-- Pablo Picasso 1881 - 1973
Outline

- Chapter 8 Topics
  - Simple logic gates (AND, OR, NOT, XOR, NAND, NOR, XNOR)
  - Multiple inputs on any simple logic gates
  - Sum-of-products design for circuits
    - Take any truth table and design a circuit using AND, OR, and NOT gates
  - DeMorgan’s Law
  - Simple circuits, such as multiplexers, full adders, half adders, decoders, encoders, and incrementors.
  - Principle behind control signal and next state circuits
  - R-S Latch, Gated D-Latch, Master-Slave flip-flop.
  - Derive a truth table from a circuit of simple logic gates
  - Transistors
    - N-type and P-type, and their operation
    - Understand and derive truth tables for transistor circuits.
    - Components of the transistor and how they affect its function
    - Moore’s Law
Find the boolean expression for \textit{Output} from following truth table. The boolean expression should be in terms of A and B and in sum-of-products (SOP) form.

\begin{tabular}{ccc|c}
  A & B & C & output \\
  0 & 0 & 0 & 0 \\
  0 & 0 & 1 & 1 \\
  0 & 1 & 0 & 1 \\
  0 & 1 & 1 & 0 \\
  1 & 0 & 0 & 1 \\
  1 & 0 & 1 & 1 \\
  1 & 1 & 0 & 0 \\
  1 & 1 & 1 & 0 \\
\end{tabular}

output =
Fill out the truth table for the following boolean equation.

\[
\text{output} = ABC' + AB'C + A'B'C + A'BC' + A'B'C'
\]

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
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Implement the following boolean equation with logic gates.

output = ABC' + AB'C + A'B'C + A'BC' + A'B'C'
Implement the following boolean equation with logic gates.

\[
\text{output} = AB + A'B' + C
\]
Fill out the truth table for the logic gate level circuit below.

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De Morgan’s Laws

\(~(AB) = \neg A + \neg B\)  given by cheatsheet

\(~(XY) = \neg X + \neg Y\)  by rewriting and changing variable name

\((XY)' = X' + Y'\)  by rewriting and changing negation notation for better visualization

\((XYZ)' = X' + Y' + Z'\)  by expanding previous line to 3 terms

\(~(A+B) = (\neg A)(\neg B)\)  given by cheatsheet

\((X+Y+Z)' = X'Y'Z'\)  by applying same algorithm
Compute the negation of the following expression using DeMorgan’s Law

\[ AB'C+D'E+(A'+B)(C'+D+E') \]

Negation

\[
= (AB'C+D'E+(A'+B)(C'+D+E'))' \quad \text{by negating entire expression}
\]

\[
= (AB'C)'(D'E)'((A'+B)(C'+D+E'))' \quad \text{by applying DeMorgan’s Law on each of the 3 products}
\]

\[
= (AB'C)'(D'E')((A'+B)'+(C'+D+E'))' \quad \text{by applying DeMorgan’s Law on the rightmost product}
\]

\[
= (A'+B+C')(D+E')(AB'+CD'E) \quad \text{by applying DeMorgan’s law on each sum on the rightmost product}
\]

\[
= (A'+B+C')(D+E')(AB'+CD'E) \quad \text{by removing unnecessary parentheses}
\]
Compute the negation of the following expression using DeMorgan’s Law

\((A'+B+C')(D+E')(AB'+CD'E)\)

**Negation**

\[= ((A'+B+C')(D+E')(AB'+CD'E))' \text{ by negating entire expression} \]

\[= (A'+B+C')'+(D+E')'+(AB'+CD'E)' \text{ by applying DeMorgan’s Law on each of the 3 sums} \]

\[= (AB'C)+(D'E)+((AB')(CD'E))' \text{ by applying DeMorgan’s Law on each sum} \]

\[= (AB'C)+(D'E)+((A'+B)(C'+D+E')) \text{ by applying DeMorgan’s law on each product on the rightmost sum} \]

\[= AB'C+D'E+(A'+B)(C'+D+E') \text{ by removing unnecessary parentheses,} \]

which matches our original expression
What is the difference between a latch and a flip-flop?
If the figure on the left is a (musical) conductor, then what is the figure on the right?
Multiple Choice Question

What does 22nm transistors mean?

a. the channel length is 22nm
b. the distance between source and drain is 22nm
c. the technology node is 22nm
d. all of the above
e. none of the above
Transistor Behavior

What are the three terminals on a transistor?

How does a transistor (pmos) function when it is ON?
Fill out the truth table for the following circuit

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What is Dennard Scaling?