CS/ECE 252
Exam 4 Review

11AM section
2015 December 11

Before we get started

Homework 8 due at beginning of lecture
Exam 4 on Monday, December 14th, during class
Today: Exam 4 Review
(Extra) office hours for HW8 and Exam4:

Dec 9th: Wednesday 12PM - 1PM in CS6367
Dec 9th: Wednesday 2:30PM - 3:30PM in CS7367
Dec 10th: Thursday 11AM - 4PM (possibly 5PM) in CS7367
Dec 10th: Thursday 12:45PM - 2:15PM in CS1308
Dec 11th: Friday 8AM - 8PM (minus class time) in CS1308
Dec 11th: Friday 12PM - 1PM in CS6367
Dec 11th: Friday 1PM - 2:30 in CS6352
Dec 11th: Friday 2:30PM - 3:30PM in CS7367
Dec 14th: Monday 8AM - 10AM in CS1308
Dec 14th: Monday 9:30AM - 11AM in CS1240

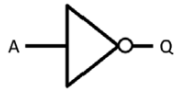
Quote of the day:

"Inspiration exists, but it has to find you working"

-- Pablo Picasso 1881 - 1973

Cheatsheet

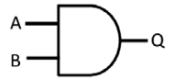
NOT GATE



A	Q
0	1
1	0

Text notation: ~

AND GATE



A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

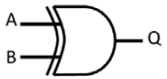
Text notation: ·

OR GATE

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

Text notation: +

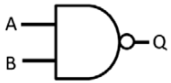
XOR GATE



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

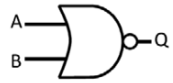
Text notation: ⊕

NAND GATE



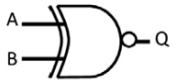
A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE



A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

XNOR GATE



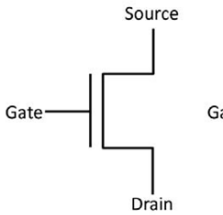
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Using other gates

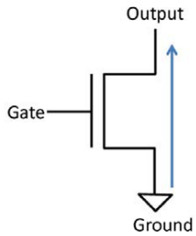
De Morgan's law

$$\sim(A \cdot B) = \sim A + \sim B$$
$$\sim(A + B) = (\sim A)(\sim B)$$

Transistor terminals

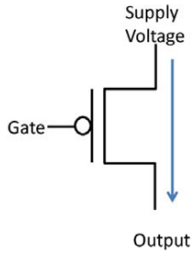


N-type transistor



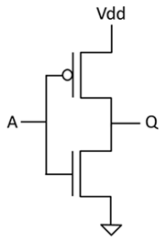
Gate	Behavior
1	Closed Output=0
0	Open Output=Z

P-type transistor

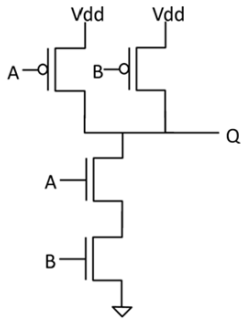


Gate	Behavior
0	Closed Output=1
1	Open Output=Z

NOT

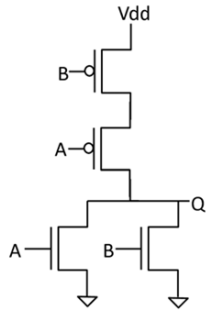


NAND



NAND Gate

NOR



NOR Gate

Outline

Chapter 8 Topics

Simple logic gates (AND, OR, NOT, XOR, NAND, NOR, XNOR)

Multiple inputs on any simple logic gates

Sum-of-products design for circuits

Take any truth table and design a circuit using AND, OR, and NOT gates

DeMorgan’s Law

Simple circuits, such as multiplexers, full adders, half adders, decoders, encoders, and incrementors.

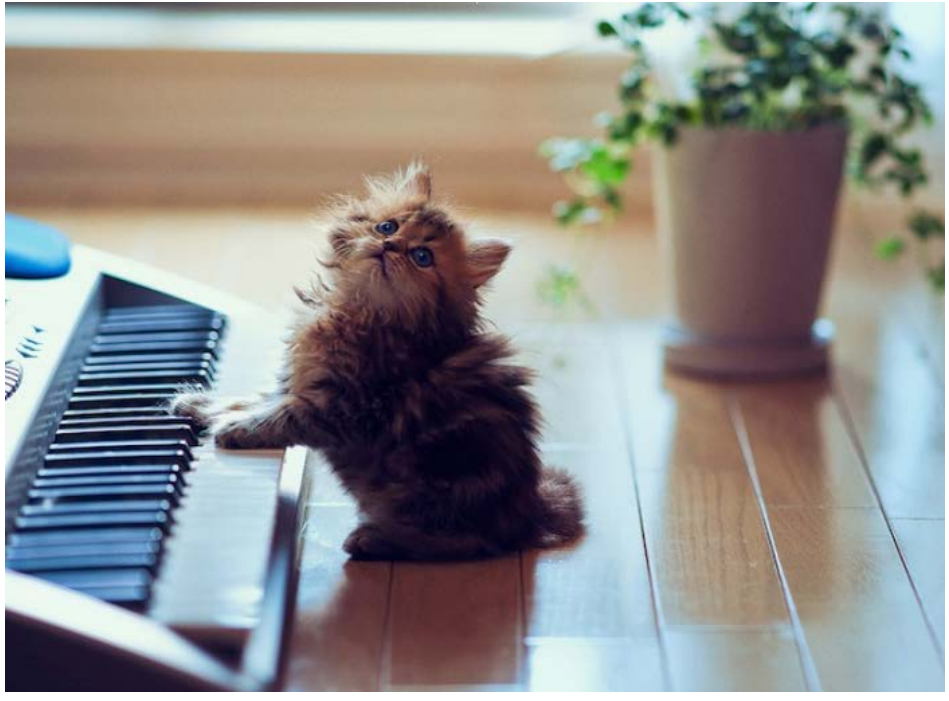
Principle behind control signal and next state circuits

R-S Latch, Gated D-Latch, Master-Slave flip-flop

Find the boolean expression for *Output* from following truth table. The boolean expression should be in terms of A and B and in sum-of-products (SOP) form.

A	B	C	output
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

output = A’B’C+A’BC’+AB’C’+AB’C



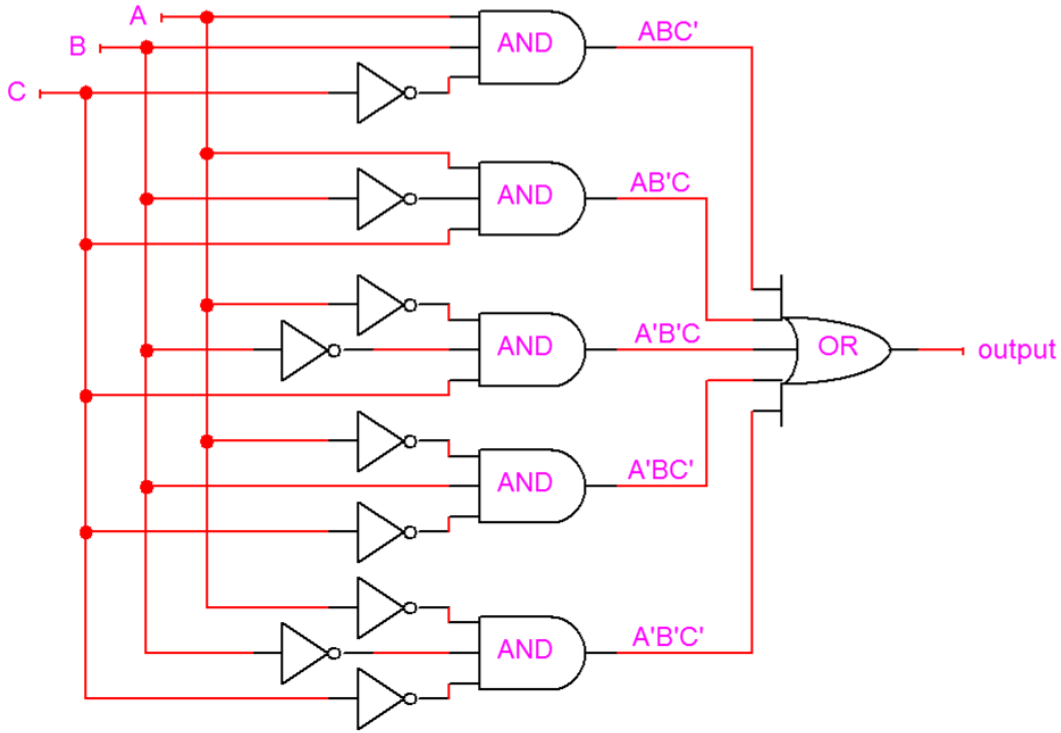
Fill out the truth table for the following boolean equation.

output = ABC’+AB’C+A’B’C+A’BC’+A’B’C’

A	B	C	output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

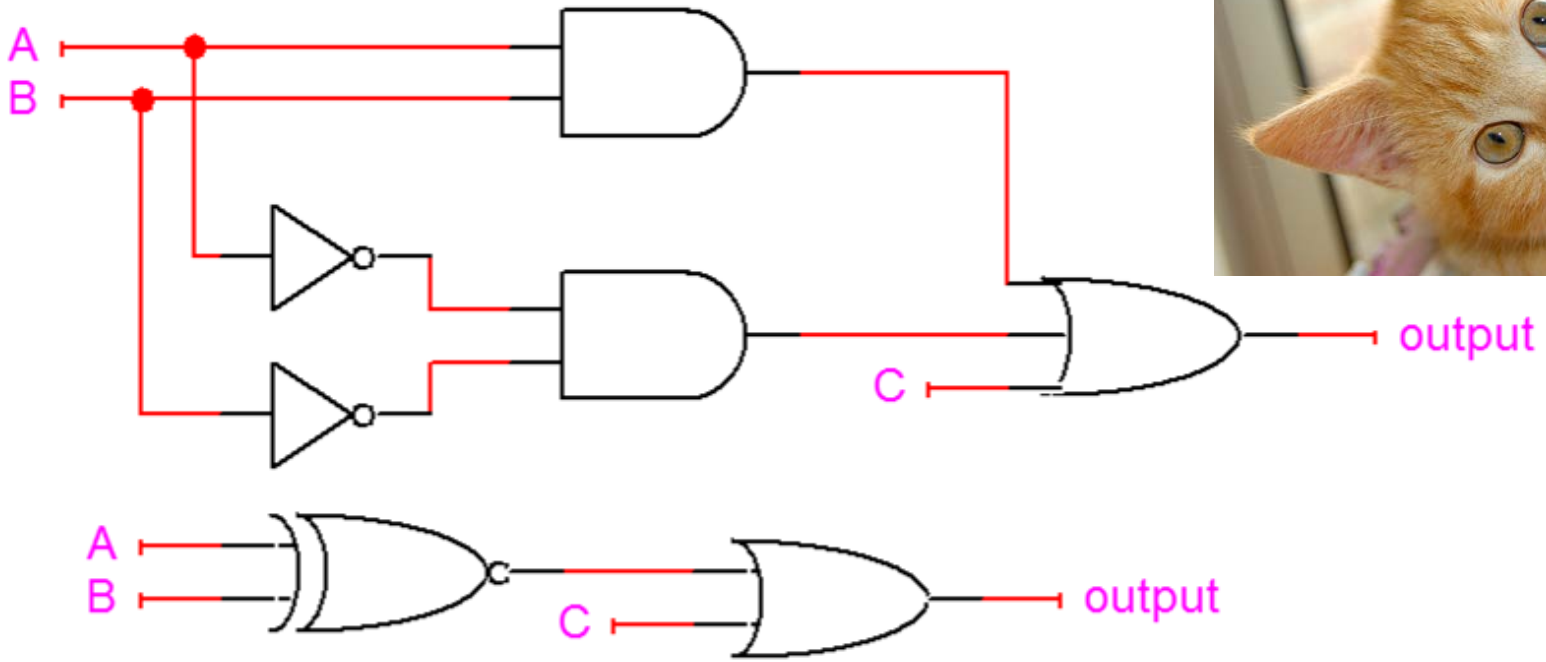
Implement the following boolean equation with logic gates.

output = ABC’+AB’C+A’B’C+A’BC’+A’B’C’

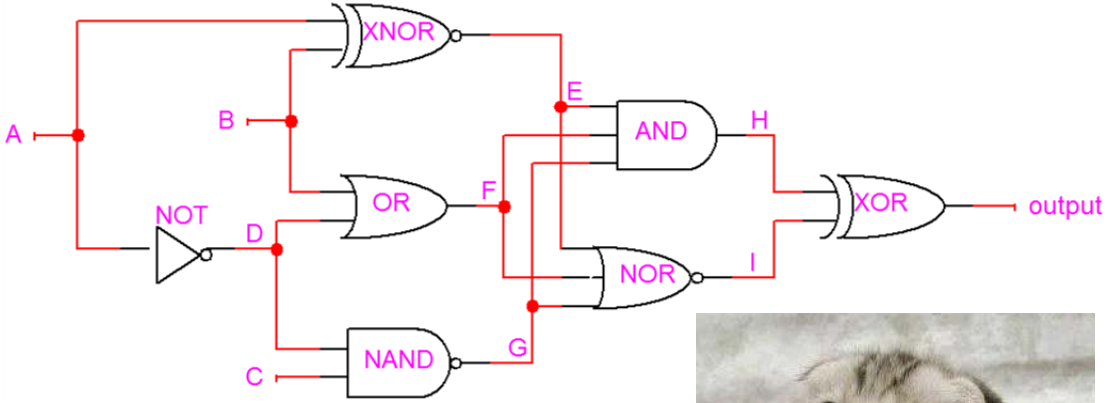


Implement the following boolean equation with logic gates.

output = AB+A’B’+C



Fill out the truth table for the logic gate level circuit below.



A	B	C	D	E	F	G	H	I	output
0	0	0	1	1	1	1	1	0	1
0	0	1	1	1	1	0	0	0	0
0	1	0	1	0	1	1	0	0	0
0	1	1	1	0	1	0	0	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	1	0	0	0
1	1	0	0	1	1	1	1	0	1
1	1	1	0	1	1	1	1	0	1

De Morgan's Laws

~(AB) = ~A + ~B	given by cheatsheet
~(XY) = ~X + ~Y	by rewriting and changing variable name
(XY)' = X' + Y'	by rewriting and changing negation notation for better visualization
(XYZ)' = X' + Y' + Z'	by expanding previous line to 3 product terms
~(A+B) = (~A)(~B)	given by cheatsheet
(X+Y+Z)' = X'Y'Z'	by applying same algorithm

Compute the negation of the following expression using DeMorgan's Law

AB'C+D'E+(A'+B)(C'+D+E')

Negation

= (AB'C+D'E+(A'+B)(C'+D+E'))' by negating entire expression

= (AB'C)'(D'E)'((A'+B)(C'+D+E'))' by applying DeMorgan's Law on each of the 3 products

= (AB'C)'(D'E)'((A'+B)'+(C'+D+E')') by applying DeMorgan's Law on the rightmost product

= (A'+B+C')(D+E')((AB')+(CD'E)) by applying DeMorgan's law on each sum on the rightmost product

= (A'+B+C')(D+E')(AB'+CD'E) by removing unnecessary parentheses

Compute the negation of the following expression using DeMorgan's Law

(A'+B+C')(D+E')(AB'+CD'E)

Negation

= ((A'+B+C')(D+E')(AB'+CD'E))' by negating entire expression

= (A'+B+C')'+(D+E')'+(AB'+CD'E)' by applying DeMorgan's Law on each of the 3 sums

= (AB'C)+(D'E)+((AB')'(CD'E)') by applying DeMorgan's Law on each sum

= (AB'C)+(D'E)+((A'+B)(C'+D+E')) by applying DeMorgan's law on each product on the rightmost sum

= AB'C+D'E+(A'+B)(C'+D+E') by removing unnecessary parentheses,

which matches our original expression

What is the difference between a latch and a flip-flop?

A flip-flop is edge triggered while latch isn’t.

If the figure on the left is a (musical) conductor, then what is the figure on the right?

semiconductor

Multiple Choice Question

What does 22nm transistors mean?

a. the channel length is 22nm

b. the distance between source and drain is 22nm

c. the technology node is 22nm

d. all of the above (correct answer)

e. none of the above

Transistor Behavior

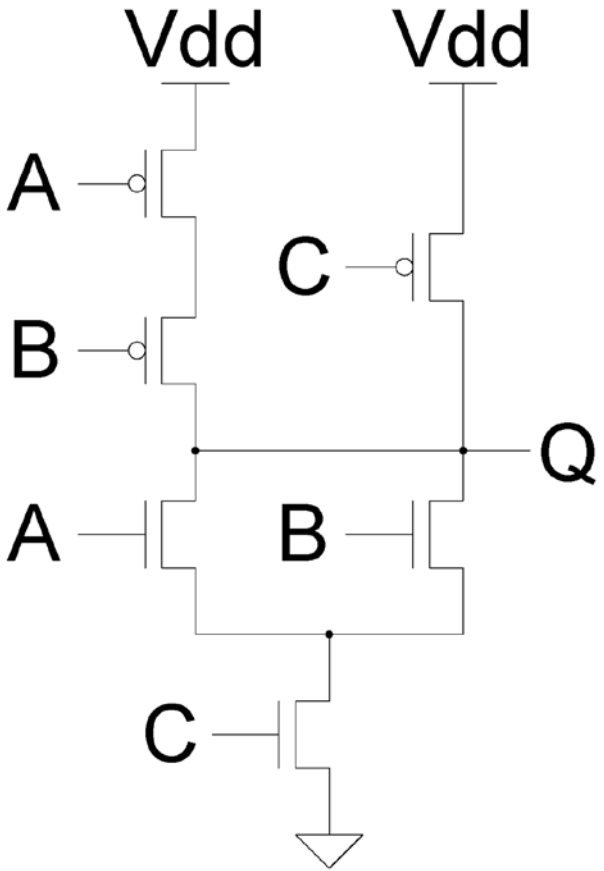
What are the three terminals on a transistor?

Gate, Source, Drain

How does a transistor (pmos) function when it is ON?

Voltage (Vdd) is applied to the gate. An electric field is created so that electrons on the other side of the insulator create a channel, so that electrons can flow from the source to the drain.

Fill out the truth table for the following circuit



A	B	C	Q
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

What is Dennard Scaling?

Dennard scaling states that voltage scales down as length/size decreases.

Supply voltage is also acceptable

Voltage and/or current is also acceptable

Power density stays constant as transistor size scales is also acceptable

Power is proportional to area is also acceptable