CS/ECE 252 HOMEWORK #4 SOLUTION
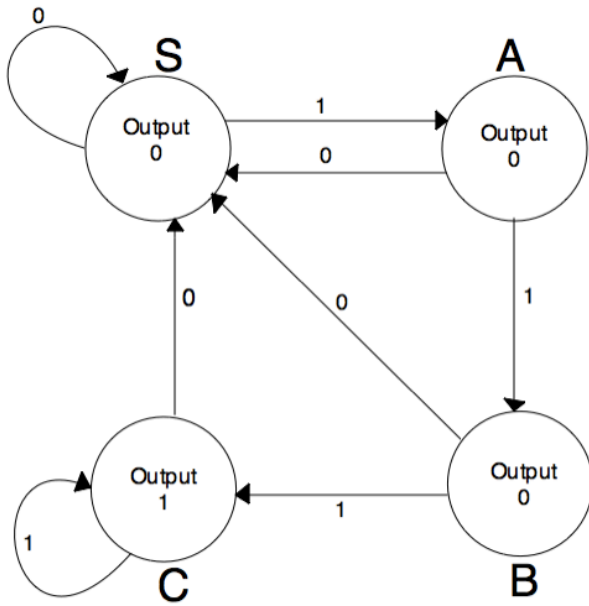
Problem 1 (8 points)
Design a finite state machine that recognizes the particular pattern "111". The input to a finite state machine (FSM) is a sequence of binary bits in series. When the FSM sees three 1's in a row, it it should output "1" - otherwise it should output a "0".

a. Create a finite state machine that recognizes consecutive patterns. For example (reading bits left to right):

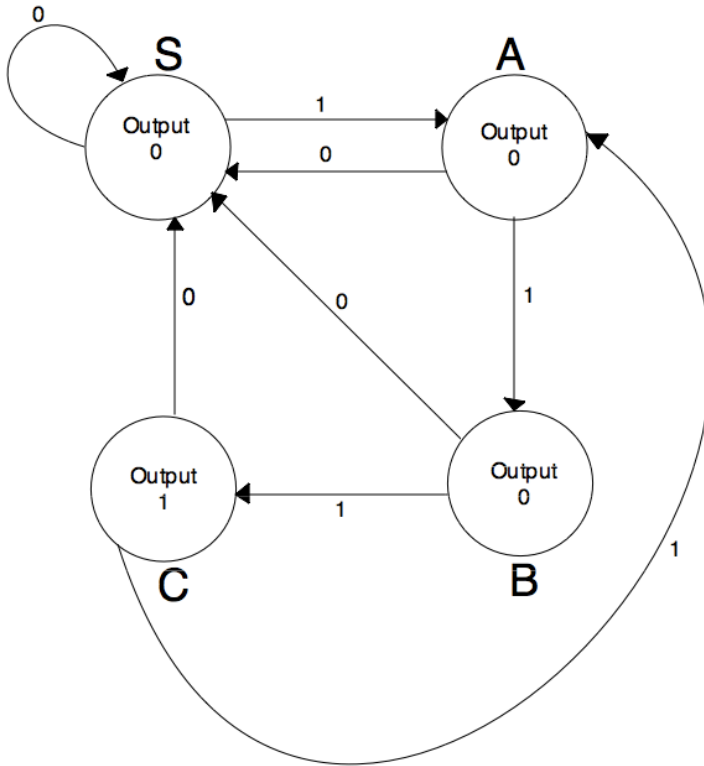input sequence -> 011110010
FSM output -> 000110000

That is, when the previous three bits in the input were "1" it outputs a 1. In this situation, it happened twice.

The start state is S.

b. Create a finite state machine that would reset and look for a new series of three 1's after it sees a
    "111" pattern. For example,

    input sequence -> 011110111
    FSM output -> 000100001

The start state is S.

Problem 2 (8 points)
The following table represents a small memory. Refer to this table for the following questions:

Address	Data
0000	1111 1111 0010 0100
0001	1100 0000 0100 0000
0010	0010 1001 0000 0101
0011	0000 0000 0101 0001
0100	0110 0010 1000 1010
0101	0110 1110 0110 1111
0110	0000 0000 0000 0010
0111	1110 0101 1101 0110

a. What binary value does location 4 contain? Location 7?
  Location 4: 0110 0010 1000 1010 in binary or x682A in hex
  Location 7: 1110 0101 1101 0110 in binary or xE5D6 in hex

b. Interpret location 0 as a two's complement integer.
  -220

c. Interpret location 5 as an ASCII value.
  no

d. Interpret location 3 as an unsigned integer.
  81

e. In the von Neumann model, the contents of a memory location can be interpreted as an instruction.
   If the binary patterns in location 1 and location 4 were interpreted as a LC-3 instruction, what
   instructions would they represent?
  Location 1: JMP R1
  Location 4: LDR R1 R2 #10

f. A binary value can also be interpreted as a memory address. If the value stored in location 6 is a
   memory address, to which location does it refer? What binary value is stored in that memory
   location?
   Location 6 refers to location 2, which contains binary value 0010 1001 0000 0101.

Problem 3 (6 points)
Suppose a 64-bit instruction takes the following format:

OPCODE	SR	DR	IMM

There are 237 opcodes and 64 registers.

  a. What is the minimum number of bits required to represent an OPCODE?
   237 opcodes < 256 = 2^8   8 bits opcode

  b. What is the minimum number of bits required to represent a register?
   64 registers = 2^6   6 bits opcode

  c. What is the maximum number of bits that can be used to represent the immediate field (IMM)?
   64 - 8 - 6 - 6 = 44 bits IMM

  d. If the immediate (IMM) uses two's complement representation, what is its maximum range of
     values?
   IMM ranges from -(2^43) to (2^43)-1, or -8796093022208 to 8796093022207

Problem 4 (4 points)
Write the operations that occur in each phase of the instruction cycle for the LDR instruction.

FETCH: Load MAR with PC, and increment PC.

       Fetch instruction (LDR) in memory and place it into MDR.

       Load IR with contents of MDR.

DECODE: Take the OPCODE and identify the LDR instruction.

EVALUATE ADDRESS: Calculate LDR source memory address by adding the base offset to the contents
of the source register.

FETCH OPERANDS: Load MAR with LDR source memory address calculated by EVALUATE ADDRESS.

                 Read from memory.

                 Place source operand into MDR.

EXECUTE: Skipped.

STORE RESULT: Write result into its designated destination.

Problem 5 (4 points)
Problem 4.14 on page 113 of ItCS.

At FETCH phase, PC = x36A2 (from Example 4.5), IR is loaded with the JMP instruction and the PC is
incremented to x36A3. At the EXECUTE phase, PC is loaded with the new value from the content of R3
(x369C). At the next instruction cycle, the processor will start executing at address x369C.