# CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

# UNIVERSITY OF WISCONSIN—MADISON

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*Midterm Examination 2*

*In Class (50 minutes)*

*Friday, October 25, 2013*

*Weight: 17.5%*

<u>**NO: BOOK(S), NOTE(S), OR CALCULATORS OF ANY SORT.**</u>

The exam has 8 pages. **Circle your final answers**. Plan your time carefully since some problems are longer than others. You **must turn in the pages 1-8**. Use the blank sides of the exam for scratch work.

LAST NAME: _____

FIRST NAME: _____

ID# _____

| Problem | Maximum Points | Points Earned |
|---------|----------------|---------------|
| 1 | 5 | |
| 2 | 2 | |
| 3 | 4 | |
| 4 | 4 | |
| 5 | 2 | |
| 6 | 5 | |
| 7 | 3 | |
| 8 | 2 | |
| 9 | 3 | |
| Total | 30 | |

**Problem 1** (5 Points)

For the following questions, select the **best** answer. Choose only **one answer per question**.

i.    What is the **addressability** (number of bytes per memory location) of a 1024 byte memory which uses 8 bits for each memory address?
    a.  2 bytes
    b.  4 bytes
    c.  256 bytes
    d.  512 bytes.

ii.   How many **transistors** are required to build a 2-input AND gate?
    a.  3
    b.  4
    c.  5
    d.  6

iii.  Which of the following can be used to distinguish **instructions** from **data**?
    a.  The number of bits used to represent them
    b.  The special format they follow
    c.  Both a and b
    d.  They cannot be distinguished

iv.   Which of the following **phases of the instruction cycle** are necessary for the processing of all instructions?
    a.  EXECUTE
    b.  EVALUATE ADDRESS
    c.  DECODE
    d.  None of the above

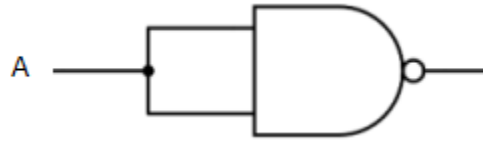v.    Which of the following is the **logic equation** for Z in the following diagram?

    a.  Z = A AND B
    b.  Z = NOT(A) AND B
    c.  Z = A AND NOT(B)
    d.  Z = A NOR B



3
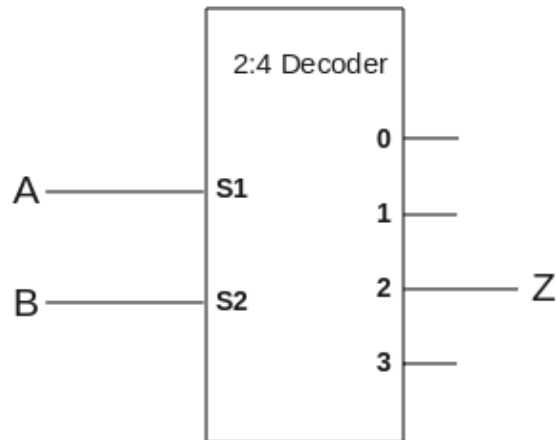
## Problem 2                                            (2 Points)

Implement **NOT(A)** using a **2-input NAND** gate.
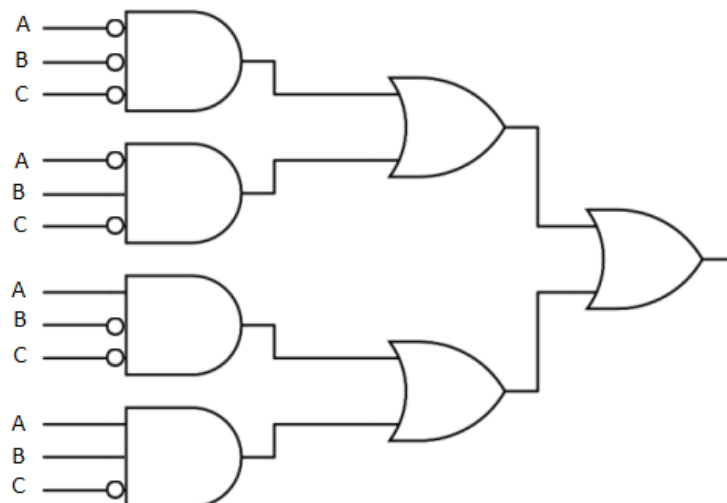


## Problem 3                                            (4 Points)

For the following truth table, with A, B and C as inputs and Z as the output, draw the gate level circuit using **3-input AND** gates, **2-input OR** gates and **NOT** gates.
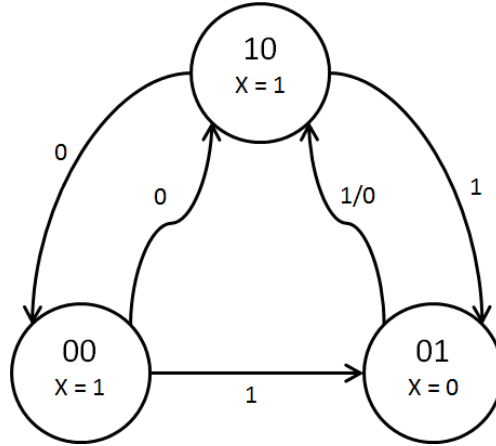
| A | B | C | Z |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

## Problem 4 (4 Points)

Complete the **Next State truth table** and the **Output truth table** for the following Finite State Machine (FSM). Each state is represented as $S_1S_0$. For example, the state marked as "10" has $S_1 = 1$ and $S_0 = 0$. X is the output in each state. $S_1'S_0'$ represents the next state.



**Next State Truth Table**

| $S_1$ | $S_0$ | IN | $S_1'$ | $S_0'$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 |

**Output Truth Table**

| $S_1$ | $S_0$ | X |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |

## Problem 5 (2 Points)

For the following logic circuit, write the **logic expression** of Z in terms of A, B and C. [e.g.: (W AND (NOT X)) OR Y].
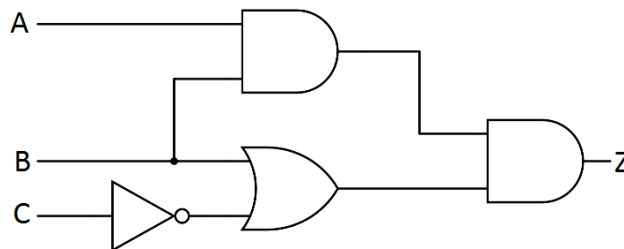


Z = (A AND B) AND (B OR NOT(C))

**Problem 6**                                                                  **(5 Points)**

Consider a vending machine which delivers a package of cookies after 15 cents are deposited. It has a single coin slot which accepts only **dimes (D) (10 cents)** or **nickels (N) (5 cents)**. Once the sum reaches (or exceeds) 15 cents a cookie is delivered. If the sum exceeded 15 cents (for example you input 2 dimes), you also get back 5 cents.

The **Finite State Machine (FSM)** is defined as follows:
**Inputs:** [Only one of D and N can be one in a clock cycle]
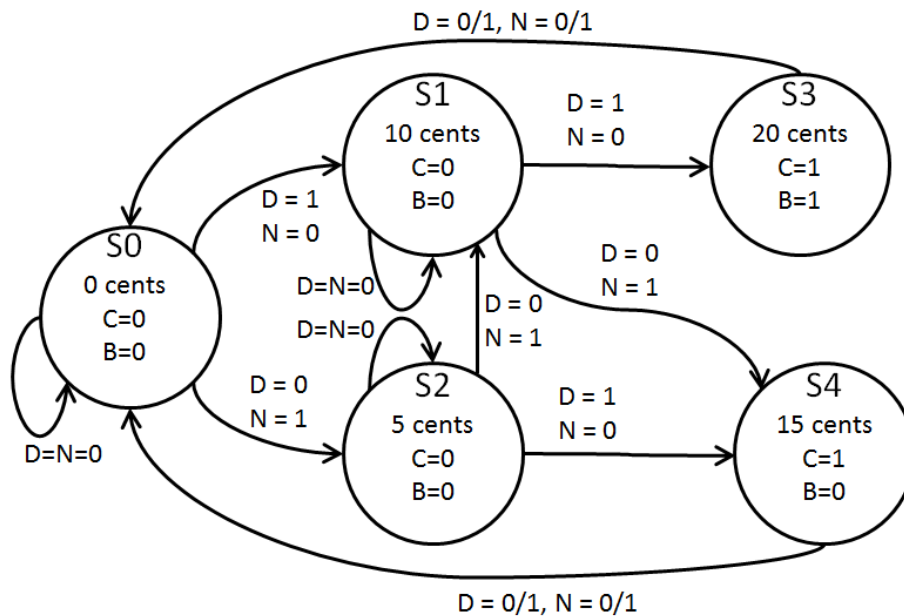    D=1 implies one dime (10 cents) was deposited
    N=1 implies one nickel (5 cents) was deposited
**Outputs:**
    C=1 implies cookie to be delivered
    B=1 implies 5 cents to be given back

a.  Complete the **state diagram** for the vending machine. Clearly show the input that causes each state transition, and output at each state.                                **(4 Points)**
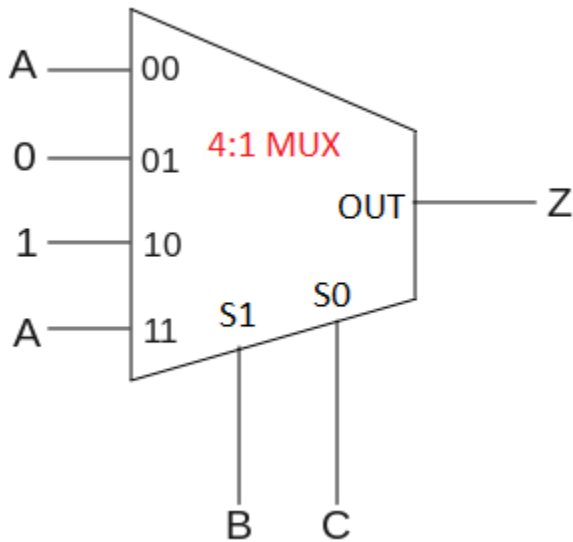


b.  How many **flip-flops (storage elements)** will be needed to implement the finite state machine designed in (a)?                                **(1 Point)**

5 states = 3 flip-flops

6

## Problem 7 (3 Points)

Complete the truth table for the following combinational circuit that uses a 4:1 multiplexer, and has A, B, C as the inputs and Z as the output.
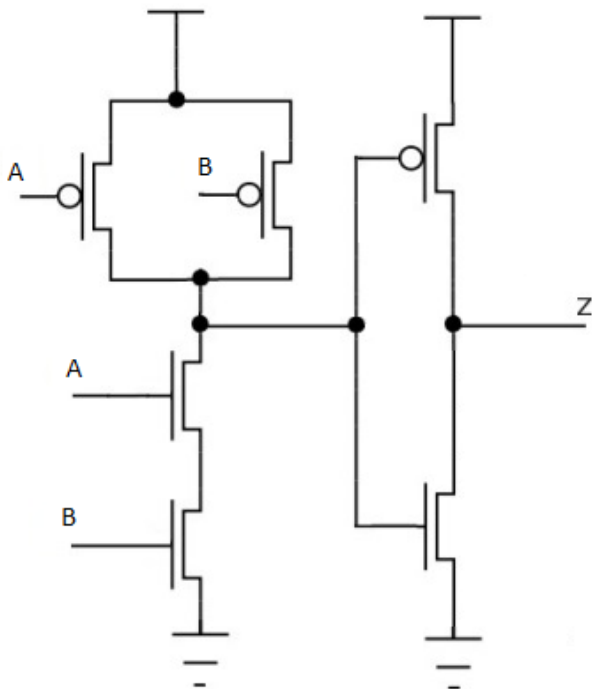


| A | B | C | Z |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

## Problem 8 (2 Points)

Complete the truth table for the following transistor-level circuit, where A, B, C are inputs and Z is the output.



| A | B | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Problem 9**                                                                                   **(3 Points)**

Answer the following questions **briefly** (1 or 2 sentences)

a.   Mention two important things that happen during the **FETCH** phase of the instruction
cycle.                                                                                    **(1 Point)**

Load instruction pointed to by PC into IR
Increment Pc to point to the next instruction

b.   What are the two components of an **instruction**?                      **(1 Point)**

Opcode: operation to be performed
Operands: data/locations to be used for operation

c.   What is the role of the **Control Unit** in the von-Neumann model?    **(1 Point)**

Orchestrates the execution of the program