CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

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Midterm Examination 2

In Class (50 minutes)

Friday, March 5, 2010

Weight: 17.5%

CLOSED BOOK, NOTE, CALCULATOR, PHONE, & COMPUTER.

The exam has **five** two-sided pages. **Circle your final answers.**

Plan your time carefully, since some problems are longer than others.

NAME: _____

SECTION: _____

ID# _____

Problem Number	Maximum Points	Actual Points
1	3	
2	4	
3	2	
4	4	
5	2	
6	2	
7	6	
8	4	
9	3	
Total	30	

Problem 1 (3 points)

Write the Boolean expression for X (in terms of A, B, and C) corresponding to the truth table shown below. You don't need to reduce the expression.

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

X = (~A & ~B & ~C) OR (~A & B & C) OR (A & ~B & C) OR (A & B & ~C)

Problem 2 (4 points)

Assume that there are 200 opcodes and 32 registers in an Instruction Set Architecture (ISA). Suppose the format of a 40 bit instruction is as follows:

OPCODE	Destination Register (DR)	Source Register (SR)	MISC

a. (1 point) What is the minimum number of bits required to represent OPCODE?

   $2^8 = 256$.

   Answer = **8 bits**

b. (1 point) What is the minimum number of bits required to represent the DR/SR?

   $2^5 = 32$.

   Answer = **5 bits**

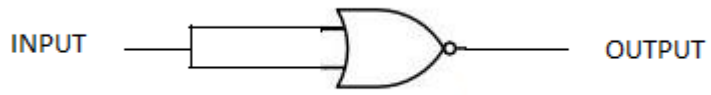
c. (2 points) Assuming the values that you computed in parts (a) and (b), what is the range of numbers that MISC can represent (assume two's complement representation)?

   Maximum bits allowed for MISC = 40 – (8 + 5 + 5) = 22

   Range of numbers allowed is from **-2^{21} to $2^{21} - 1$**.

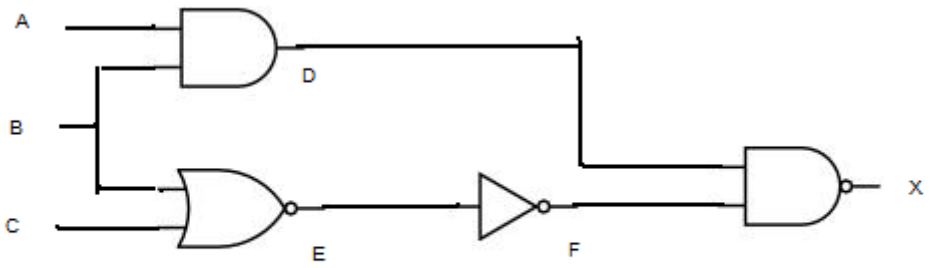
Problem 3 (2 points)

Show how to implement a NOT gate using a two input NOR gate.



Problem 4 (4 points)

In the combinational circuit shown below, A, B, and C are the inputs and X is the output. D, E, and F are internal nodes.



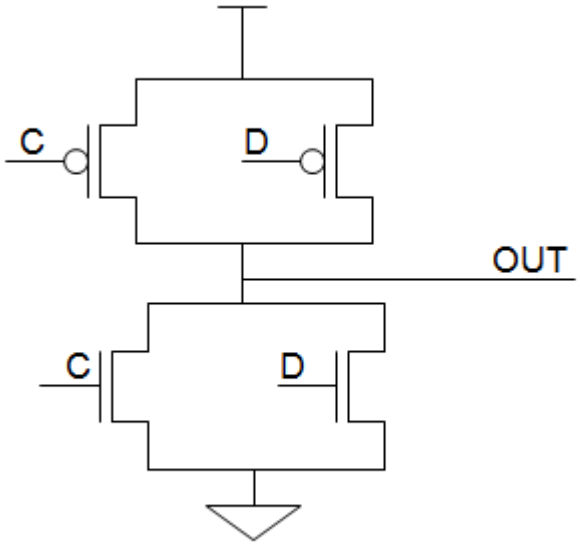
a. (2 points) What are the values of D, E, F, and X when A = 0, B = 1, C = 1?

D = 0 E = 0 F = 1 X = 1

b. (2 points) What is the value of X when A = 1 and B = 1?

When A = B = 1, D is 1. Also, when B = 1, E = 0 (since the output of a NOR gate is 0 if at least one of its inputs is 1). So F = 1. And X has to be **0** (since the output of a NAND gate is 0 when both its inputs are 1).

Problem 5 (2 points)



The circuit shown above (C and D are the inputs and OUT is the output) has a major flaw. What is it? *Hint*: Evaluate the circuit for all sets of inputs.

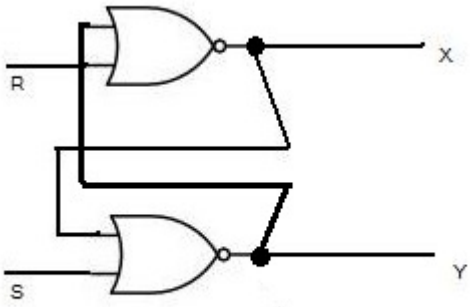
Consider what happens when the inputs C and D are not equal, say C = 0, and D = 1. In this case, both 1 and 0 come to the OUT node. Hence there is a short in the circuit, which is an invalid construction of the circuit.

Problem 6 (2 points)

A two input AND and a two input OR are both examples of two input logic functions. How many different two input logic functions are possible? Explain your answer (No credit without explanation).

For two input logic functions, the number of rows in the truth table is $2^2 = 4$. Each of these rows can be filled with a 0 or 1 (independently) to generate unique logic functions. So the answer is $2^4 =$ **16**.

Problem 7 (6 points)



a. (2 points) For this RS latch, what are the values of X and Y, if S = 1 and R = 0?

X = 1 Y = 0

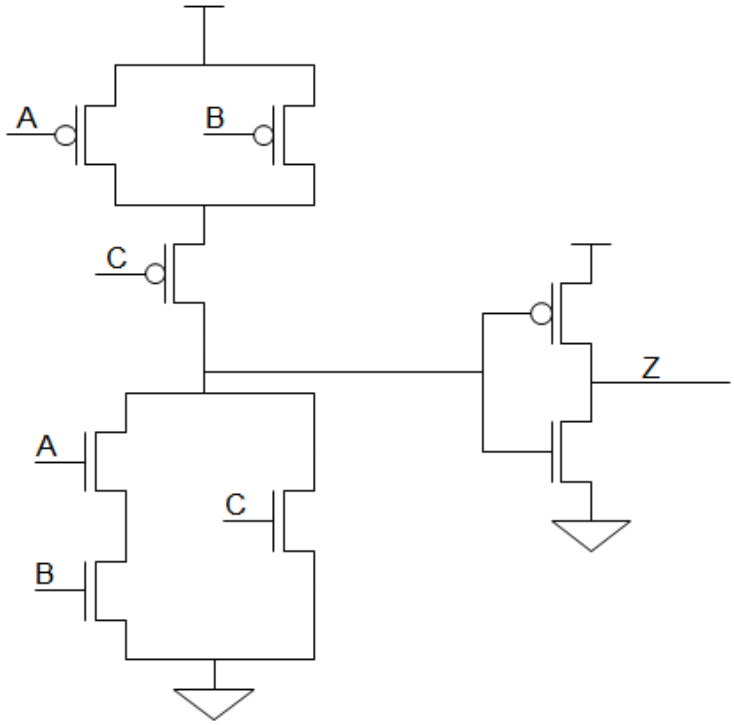
b. (2 points) Now S changes to 0 (S = R = 0). What are the values of X and Y?

X = 1 Y = 0

c. (2 points) Then R changes to 1 (S = 0 and R = 1). What are the values of X and Y?

X = 0 Y = 1

Problem 8 (4 points)



In the above circuit, A, B, and C are the inputs, and Z is the output.

a. (2 points) Find the value of Z when A = 1, B = 0, C = 0.

Intermediate output (before the final inverter) = 1

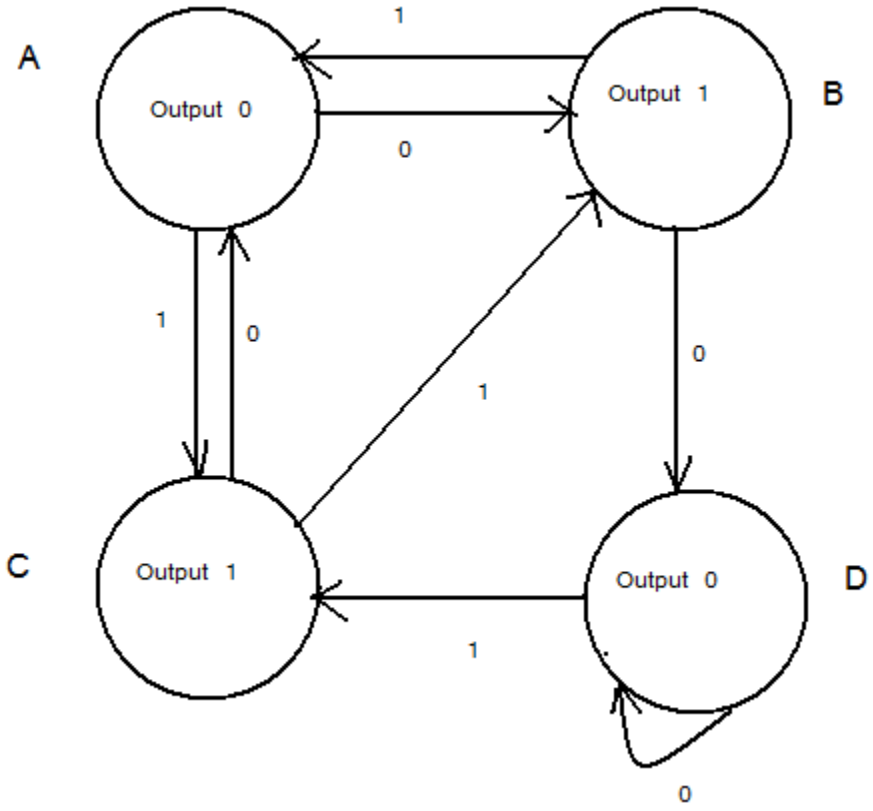
Z = NOT (1) = **0**

b. (2 points) Find the value of Z when A = 0, B = 0, C = 0.

Intermediate output (before the final inverter) = 1

Z = NOT (1) = **0**

Problem 9 (3 points)



Assume that A is the start state in the FSM shown above. Determine the output sequence and the final state when the FSM acts on the input stream 111101.

States Visited **ACBACAC**

Final State **C**

Output Sequence **0110101**

Scratch Page (in case you need additional space for some of your answers)