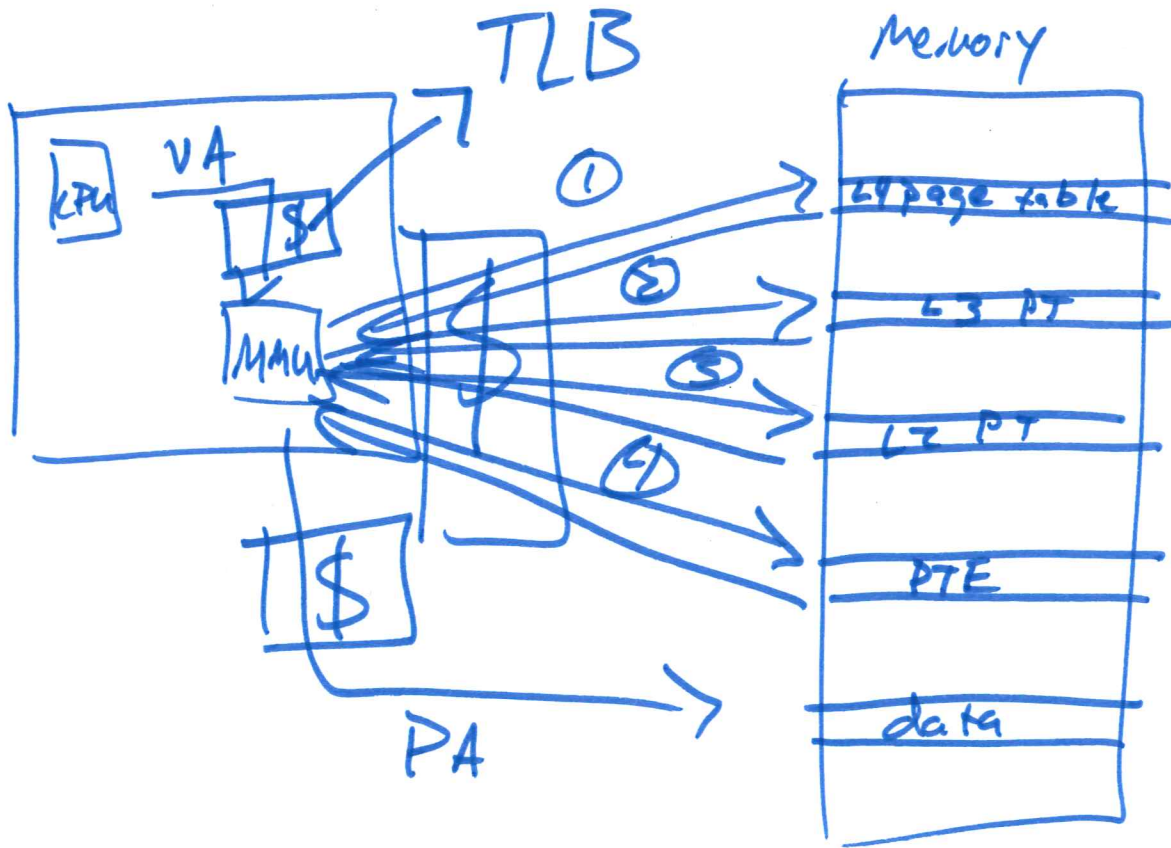


Increasing performance of address translation



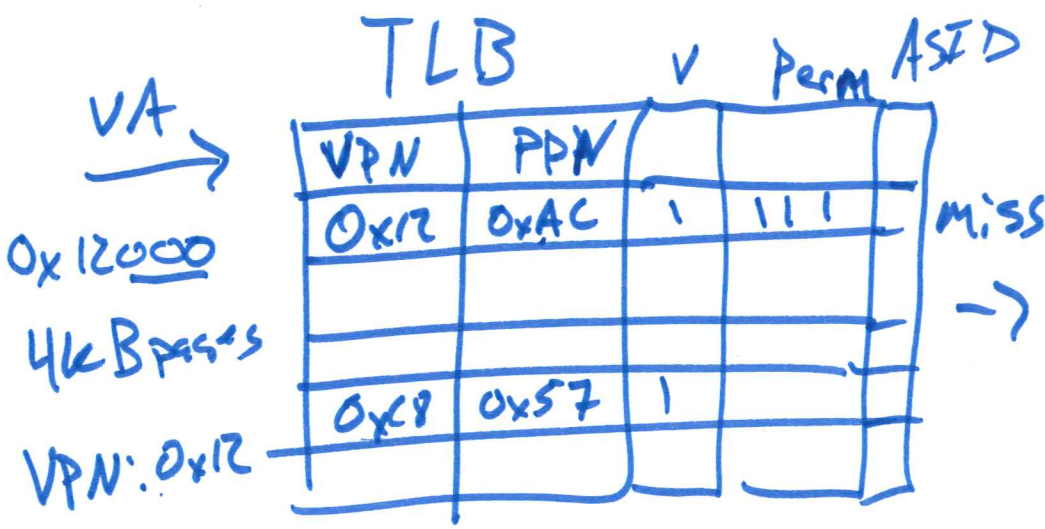
x86-64 up to 4 accesses per ld/st

Add a ~~the~~ cache

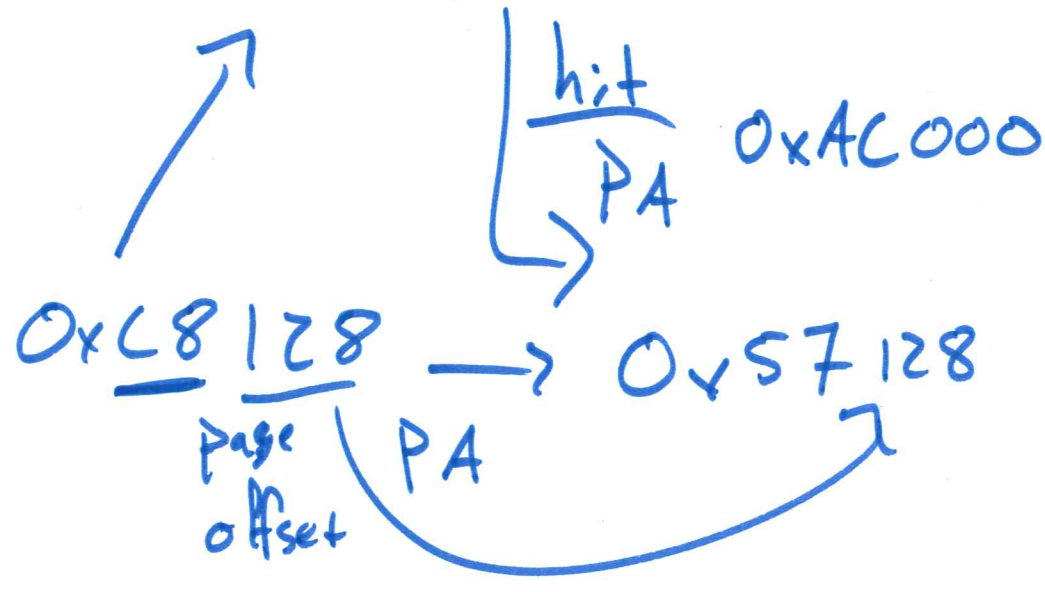
TLB → translation look-aside buffer

↳ cache our address translations

↳ indexed by virtual address



Page table walk
4 accesses to memory



if TLB is SA the bits in VPN give the set # / set index

TLB takes advantage of temporal and spatial locality

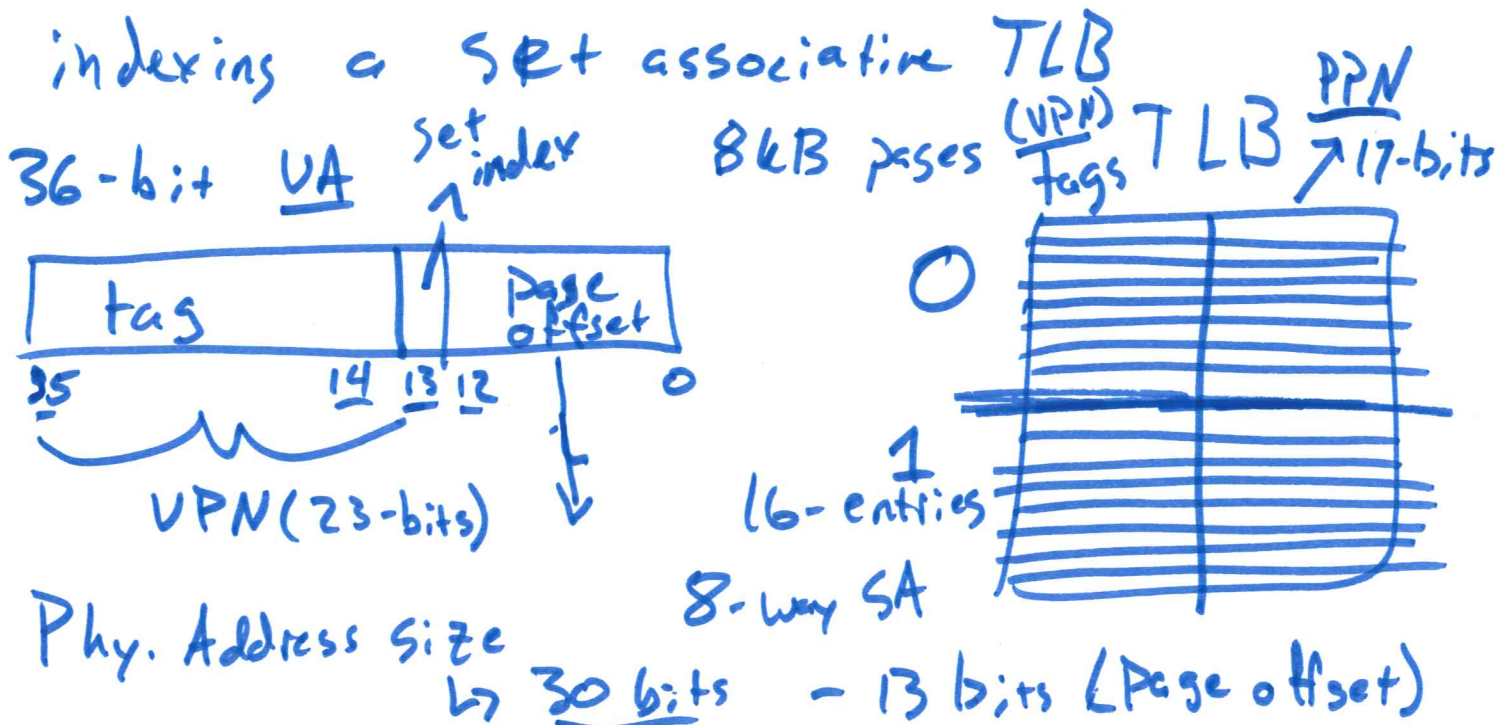
- accessing same data
- if accessing other data within the same page

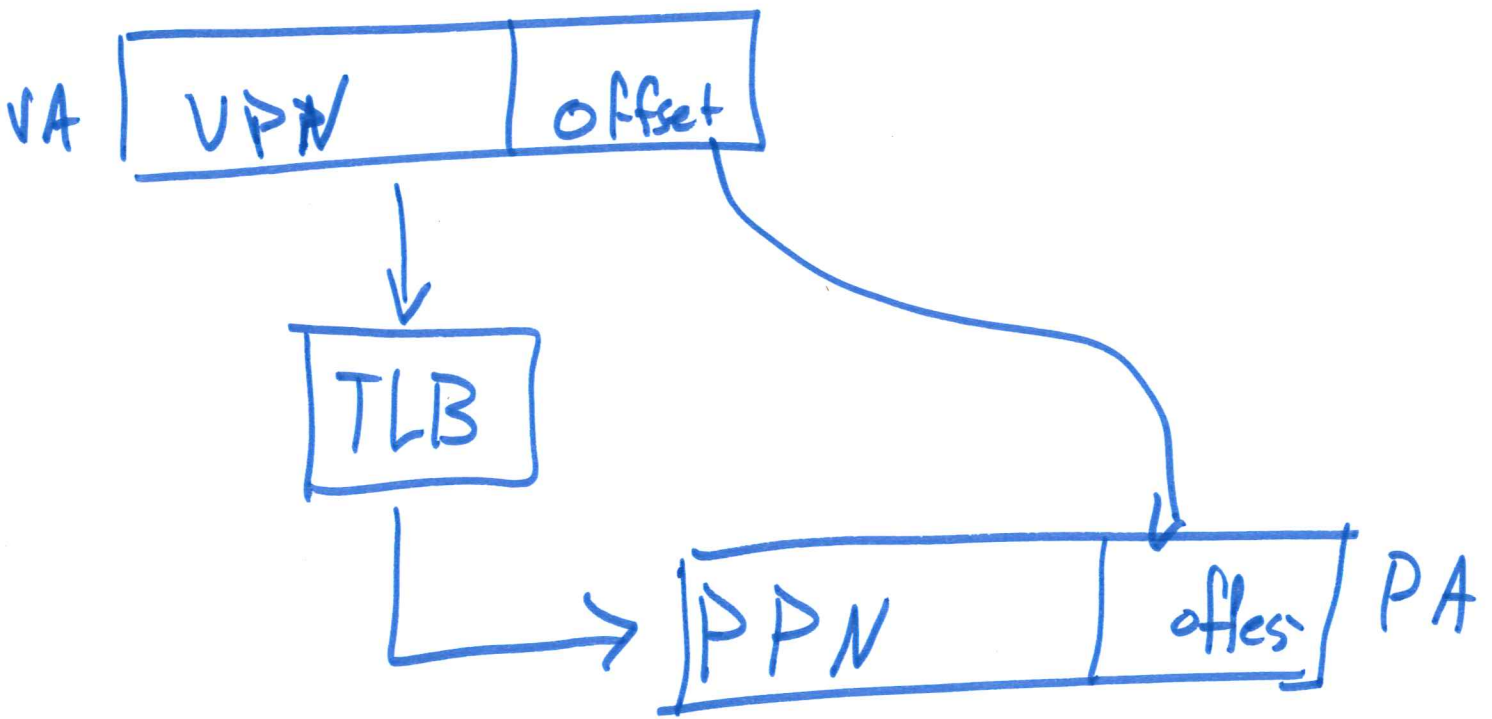
is the TLB is direct-mapped?
 Set-associative?
Fully-associative?

fully-associative \rightarrow went highest hit rate possible
 \rightarrow ~~get's~~ gets rid of all
conflict misses

TLB must be very fast
 it's on the critical path to L1 cache

TLBs are small 16-64 maybe 96
 entries





movl 0x0301004, %ebx
movl (%ebx), %ecx

$\%ecx = 71.2$
 $\%ebx = 0x00023790$

offset

VA 0: 0x03010004
VA 1: 0x00023790
VA 2: 0x
VA 3: 0x

set index
4 = 10100

PA 0: 0x03010004
PA 1: 0x00023790
PA 2: 0x
PA 3: 0x

Virtual address

Virtual page number	Page offset
31 16-5 bits	0
L2 Index	L1/PTE Index
31 8	16 15
24 23	16

Page table entry

Physical page number	Valid	Present
31 20	2	1
16-bit in Page offset	→ 36-16 = 20	

Physical Memory (shown as 4-byte words)

0x813B80000	0x7492B2F4	0x813B8000	0x813B8000
	0xD411F7D4		0x8588A11
	0x7C32B114		0x9A52511
	0xFB80E4		0xB0BB111
	0x280BA000		a b c d
	0		r l d /o
	0		o _ w o
	0xD1ACB000		h e l l
0x7A2300000	0xD1ACB000	0xB0BB10000	0.117
	0xB94E4758		0x03020010
	0xF9A7F898		0.153
	0x57691828		0x03020008
0x5E1F90000	0x986DFAEC	0xB79E50000	
	0x6336C1BC		0
	0xDDE932A4		0
	0x4368AD88		0
0x417E30000	0x525D7838	0xAC2620000	0
	0x5E1F910		10
	0xB79E511		9
	0x02C7211		8
0x280BA0000	0xAC26200	0x9A5250000	7
	0xA445B1F0		1.29
	0x1B58C68		2.8
	0x00023790		13.9
0x02C720000	0x2DB007B4	0x8588A0000	71.2

MMU

CR3 register: 0x7A2300000

VPN	PPN	V
0x0002	0x8588A	1
0x0301	0x02C72	1
0xABCD	0x741AC	1

2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages

Physical address

Cache tag	Set index	Block offset
4 3 1 3 1	0	0

Cache (4-bytes words)

V	Tag	Word 0	Word 1
1	0x8588A479	71.2	13.9
1	0x8588A400	16.7	56.0
1	0x02C72000	0x2DB007B4	0x00023790
1	0x9A525000	7	8
1	0x9A525000	9	10
1	0xB0BB1000	r l d /o	a b c d
1	0xB79E5000	0x03020010	0.117
0			

0x8588A3790

64-way SA