Curriculum Vitae

Jason Lowe-Power
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Research Interests

As a computer architect, I broadly want to enable the continuing exponential growth in computing capability despite the slowing of Moore's Law. My research interests are heterogeneous systems, memory systems, and hardware-software interaction.

Education

PhD in Computer Science, Expected May 2017
University of Wisconsin-Madison

MS in Computer Science, August 2013
University of Wisconsin-Madison

Bachelor of Science in Computer Science, May 2010
Georgia Institute of Technology *Summa cum laude*

Refereed Conference Publications

Jason Lowe-Power, Mark D. Hill, David A. Wood. "Adaptive Victim Cache: Reducing Access Amplification in a DRAM Cache." Currently under review.

Hongil Yoon, Jason Lowe-Power, Gurindar S. Sohi. "Reducing GPU Address Translation Overhead with Virtual Caching." Currently under review.

Lena E. Olson, Jason Power, Mark D. Hill, David A. Wood. "Border Control: Sandboxing Accelerators." *Proceedings of the 48th International Symposium on Microarchitecture* (**MICRO**-48). Dec 2015.

Jason Power, Mark D. Hill, David A. Wood. "Supporting x86-64 Address Translation for 100s of GPU Lanes." *Proceedings of the 20th IEEE International Symposium On High Performance Computer Architecture* (**HPCA** 20). Feb 2014.

Jason Power, Arkaprava Basu, Junli Gu, Sooraj Puthoor, Bradford M. Beckmann, Mark D. Hill, Steven K. Reinhardt, David A. Wood. "Heterogeneous System Coherence for Integrated CPU-GPU Systems." *Proceeding of the 46th International Symposium on Microarchitecture* (**MICRO**-46). Dec 2013.

Journal Publications

Jason Power, Yinan Li, Mark D. Hill, Jignesh M. Patel, David A. Wood. "Implications of Emerging 3D GPU Architecture on the Scan Primitive." *SIGMOD Rec.* 44(1). May 2015.

Jason Power, Joel Hestness, Marc S. Orr, Mark D. Hill, David A. Wood. "gem5-gpu: A Heterogeneous CPU-GPU Simulator." *Computer Architecture Letters.* 14(1). Jan-June 2015.

Refereed Workshop Publications

Jason Lowe-Power, Mark D. Hill, David A. Wood. “When to use 3D Die-Stacked Memory for Bandwidth-Constrained Big-Data Workloads.” *The Seventh Workshop on Big Data Benchmarks, Performance Optimization, and Emerging Hardware* (BPOE 7) at ASPLOS. Apr 2016.

Jason Power, Yinan Li, Mark D. Hill, Jignesh M. Patel, David A. Wood. “Toward GPUs being mainstream in analytic processing: An initial argument using simple scan-aggregate queries.” *Proceedings of the 11th International Workshop on Data Management on New Hardware* (DaMoN'15). June 2015.

Invited Talks

Jason Lowe-Power. “Programmable Accelerators.” 2016 IBM Research Workshop on Architectures for Cognitive Computing and Datacenters. Oct 2016.

Jason Power. “The Benefits of GPUs for Analytic Processing—Today and Tomorrow.” Google Tech Talk. June 2015.

Jason Power. “Supporting x86-64 Address Translation for 100s of GPU Lanes.” AMD Research. Feb 2014.

Other Talks

Jason Lowe-Power, Mark D. Hill, David A. Wood. “Bandwidth Optimized DRAM Caches.” UW Computer Architecture Affiliates Meeting. Nov 2016.

Jason Power. “Little Shop of gem5 Horrors.” Second gem5 Users Workshop with ISCA 42. Jun 2015.

Jason Power. “BitWarp: Energy Efficient Analytic Data Processing on Next Generation General Purpose GPUs.” UW Computer Architecture Affiliates Meeting. Oct 2014.

Jason Power, Mark D. Hill, David A. Wood. “MMUs for GPGPUs: Supporting x86-64 Address Translation for 100s of GPU Lanes.” UW Computer Architecture Affiliates Meeting Oct 2013.

Jason Power, Marc S. Orr. “gem5-gpu: A Simulator for Heterogeneous Processors.” First Annual gem5 User Workshop with MICRO 45. Dec 2012.

Awards

Cisco Systems Distinguished Graduate Fellowship 2015–2016

Cisco Systems Distinguished Graduate Fellowship 2014–2015

Summer Research Assistant Award Summer 2011

Teaching

Primary Lecturer, *CS 354 (Machine Organization and Programming)*. Fall 2015. University of Wisconsin-Madison.
Lectured to class of 141 three times weekly. Prepared teaching material, tests, and assignments. Teaching evaluations available upon request.

Guest Lecture: *CS 752 (Advanced Computer Architecture I)* DRAM, Memory Systems, and Virtualization. University of Wisconsin-Madison. Spring 2015.

Guest Lecture: *CS 757 (Advanced Computer Architecture II)* GPU Architectures and Memory Systems. University of Wisconsin-Madison. Spring 2014.

Teaching assistant. Honors Calculus I. Fall 2007.
Georgia Institute of Technology.
Taught class of 32 twice weekly and assisted students one-on-one.

Industry Experience

Intern at Advanced Micro Devices (AMD) Research. Spring 2012

Co-op at Georgia Tech Research Institute (GTRI). 2008–2009
Acquired Secret Security Clearance

Patents

Jason G. Power, Bradford M. Beckmann, Steven K. Reinhardt. "Serving memory requests in cache coherent heterogeneous systems." US Patent Pending, Filed Mar. 2013.

Professional Activities

External reviewer: VLSI 2014, HPCA 2015, DaMoN 2015, TACO, TODAES

Volunteer and Outreach

Scratch Club for 5th Graders Fall 2014
Taught an after-school class of 16 5th graders the basics of computer science as part of a team. Helped develop lesson plans and taught the whole class and students one-on-one.

40 Years of Computer Architecture Fall 2014
Created a poster which details professors, graduates, and their awards throughout the history of the computer architecture program at UW-Madison.