Average lifetime of microprocessors is expected to decrease ⇒ More failures on the field. Can we predict the failure?

**Virtual Aging**
- Delay Degradation ➔ Exposing Failure
  - Near-critical paths
  - Non-critical path
  - Fast gate
  - Phased CLK
  - Additional logic inserted to cover fast gates

**Objective**
- Wearout in critical paths
- Naturally exposed
- Wearout in non-critical paths
- Clock phase shifting logic

**Evaluation**
- Delay Aware Simulation
- Delay as a function of Time/V_{dd}
- Applications

**Results**
- 50mV reduction in V_{dd} to predict failures 9 months in advance

**Delay Degradation ➔ Exposing Failure**
- Slack = 70ps
- Slack = 50ps
- Slack = 20ps
- 50ps
- 40mV

**Failure ➔ Detection**
- Sampling DMR
  - Less than 1% energy overhead
  - No performance overhead
  - 100% Coverage
- FPGA acceleration
  - Full system OpenRISC processor
  - Applications – SPEC benchmarks
  - Synopsys MOSRA
  - Wearout model @ transistor level