

# Energy consumption limits in high-speed optical and electronic signal processing

R.S. Tucker, K. Hinton and G. Raskutti

The energy consumption of high-speed optical signal processing circuits using optical and electronic components is compared. Integrated nonlinear optical circuits consume more energy than CMOS ICs with O/E and E/O converters in all but the very simplest of circuits. It is concluded that future generations of high-performance electronics will be the technology of choice for optical signal processing.

**Introduction:** The processing power of digital electronic circuits continues to follow an upward trajectory [1] according to Moore's law. But to maintain this trajectory, electronic chip designers are struggling against thermal limitations caused by energy dissipation at the device [2] and interconnect [3] level. In optical communication systems the optical transmission medium (usually a fibre) has a bandwidth that greatly exceeds the bandwidth of any conceivable electronic device and the bandwidth of the optical-to-electrical (O/E) and electrical-to-optical (E/O) converters needed to interface electronic processing circuits to the optical transmission medium. This imbalance between the optical and electronic bandwidths is sometimes referred to as the 'electronic bottleneck' [4].

One could conclude from this line of reasoning that all-optical devices based on nonlinear optics may eventually replace electronics in very-high-speed signal processing systems, especially where the data to be processed is already in optical form. For example, devices such as semiconductor optical amplifiers (SOAs) [5], guided-wave devices using periodically-poled lithium niobate [6], and highly-nonlinear optical fibres (HNFs) [7, 8] might replace electronics for packet header processing, regeneration and wavelength conversion in ultra-high-bit-rate optical communications systems. However, raw processing speed is not the only factor that needs to be considered. The energy consumption of the circuit is at least as important.

In this Letter we compare the energy consumption of optical signal processing in HNF and SOA optical circuits with optical signal processing using electronic digital ICs. It is shown that electronic CMOS ICs have lower energy consumption than HNFs and SOAs if the number of operations per bit of input data is more than about 20. Therefore, in all but the very simplest of circuits, integrated nonlinear optical circuits cannot compete with CMOS ICs from a power consumption point of view. The data for electronic devices presented here applies specifically to CMOS devices, but the broad conclusions also apply to other high-performance electronic technologies. Owing to space limitations, we have not included guided-wave devices using periodically-poled lithium niobate, but the power consumption of these devices is typically larger than SOA devices.

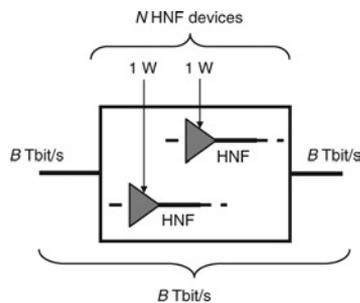


Fig. 1 Model of HNF circuit

**System model:** The analysis presented here uses the system model presented in Figs. 1-3. Fig. 1 is an optical processor based on HNF devices, Fig. 2 is an optical processor using SOA devices, and Fig. 3 is an electronic CMOS processor with accompanying O/E and E/O converters. In all three circuits, the incoming and outgoing aggregate bit rate is  $B \times 1$  Tbit/s, which is limited by the bandwidth of the input and output fibres. In the analysis presented here we will consider three values for  $B$ :  $B = 10$  (i.e. 10 Tbit/s, the maximum capacity of a fibre),  $B = 1$  (i.e. 1 Tbit/s), and  $B = 0.1$  (i.e. 100 Gbit/s).

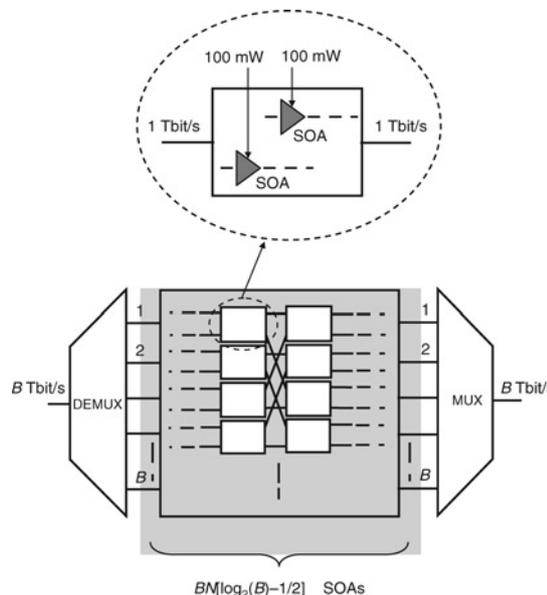


Fig. 2 Model of SOA circuit

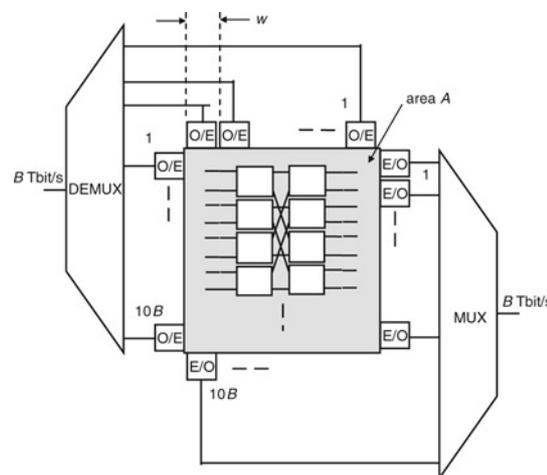


Fig. 3 Model of CMOS circuit

The HNF circuit in Fig. 1 contains  $N$  HNF devices. Although there has not been a demonstration of an HNF optical device operating at 10 Tbit/s, there have been forecasts of such high-speed operation, based on the speed of the nonlinear dynamics in HNF [9]. As pointed out earlier, the maximum bit rate is limited by the bandwidth of the input and output fibres to around 10 Tbit/s, corresponding to  $B = 10$ . To fully utilise this high-speed capability, the incoming and outgoing bit streams are on a single wavelength. All devices in the HNF circuit are assumed to operate at the full  $B$  Tbit/s speed of the incoming data and each incoming bit is operated upon by all  $N$  devices. The processing capacity of the HNF circuit is  $BN \times 10^{12}$  operations per second.

The processing speed of the SOA devices in the circuit in Fig. 2 is limited by the usable bandwidth of the SOA devices, which is around 1 THz [10]. To achieve a 10 Tbit/s processing speed using SOA devices, it is necessary to multiplex the incoming data onto a number of wavelengths, each carrying data at a lower bit rate, and to use a larger number of devices for processing. If the incoming data rate is  $B \times 1$  Tbit/s, with  $B > 1$  and given the capacity of each SOA device is 1 Tbit/s, the incoming data stream needs to be wavelength multiplexed onto  $B$  channels, as shown in Fig. 2.

To provide the same processing power as the HNF circuit ( $BN \times 10^{12}$  operations per second), the SOA circuit is constructed using a number of signal processing blocks, all interconnected using a Benes interconnection arrangement, as shown in Fig. 2. As shown in the inset to Fig. 2, each signal processing block contains  $N$  SOA devices. The Benes structure requires  $BN/2 [2\log_2(B) - 1]$  active devices and each incoming bit is operated upon by  $N [\log_2(B) - 1/2]$  active devices. If  $B \leq 1$ , only one wavelength is required in Fig. 2, and the Benes-interconnected signal processing blocks are replaced by a single

block containing  $N$  devices. All SOA devices in the circuit operate at a bit rate of 1 Tbit/s.

The maximum processing speed of the CMOS devices in the model in Fig. 3 is taken to be 100 Gbit/s. It is expected that this bit rate will be achievable in future generations of CMOS [11] and O/E and E/O converters. For  $B > 0.1$ , the incoming and outgoing data in Fig. 3 is wavelength multiplexed onto  $10B$  channels and the incoming and outgoing channels are converted from optical to electrical and electrical to optical form using  $10B$  O/E and  $10B$  E/O converters on the input and outputs of the CMOS circuit, respectively. To provide the same processing power as the HNF circuit in Fig. 1 and the SOA circuit in Fig. 2 (i.e.  $BN \times 10^{12}$  operations per second), the CMOS circuit uses signal processing blocks that are interconnected using a Benes interconnection as shown. Each block contains  $N$  CMOS devices. For  $B > 0.1$ , the Benes structure requires  $5BN [2\log_2(10B) - 1]$  active devices and each incoming bit is operated on by  $N[\log_2(10B) - 1/2]$  active devices. For  $B \leq 1$ , the Benes structure, requires  $N$  active devices.

**HNF circuits:** The power consumption of an HNF device is dominated by the optical power needed to produce a nonlinear change in the refractive index. In principle, it is possible to reduce this optical power by increasing the length of the device. But as the length is increased, fibre losses begin to dominate. The optimum optical power of typical HNF devices is of the order of 1–10 W [7, 8]. A power of 1 W is assumed in this Letter. The total energy (in joules) in all devices per bit of input/output data is

$$E_{\text{HNF}} = \frac{N \times 10^{-12}}{B} \quad (1)$$

**SOA circuits:** The power consumption of an SOA device is dominated by the electrical drive power required to produce gain in the active region. Although SOAs typically consume 200 mW or more, it is assumed conservatively here that the drive power for each SOA device is 100 mW [11]. The total energy (in joules) in all devices per bit of input/output data is therefore

$$E_{\text{SOA}} = N \left[ \log_2(B) - \frac{1}{2} \right] \times 10^{-13} \quad B > 1$$

$$E_{\text{SOA}} = \frac{N \times 10^{-13}}{B} \quad B \leq 1 \quad (2)$$

**CMOS circuits:** There are three key contributions to the energy consumption of the CMOS circuit: (a) the O/E and E/O converters, (b) the CMOS devices, and (c) the interconnecting wires between devices. In the calculations presented here, the energy consumption in the O/E and E/O converters is taken to be 0.5 mW/Gbit/s (i.e. 0.5 pJ/bit). This figure was obtained by extrapolating a figure of 2.5 mW/Gbit/s (in 80 nm CMOS) reported in [12]. The energy per bit is taken as 0.1 fJ/bit in each of the CMOS devices [1], and  $0.5C_iV^2$  in the wires, where the wire capacitance is  $C_i = 0.1$  fF/ $\mu\text{m}$  [1], the average interconnect wire length per device is  $L_i = 5d$  where  $d$  is the average spacing between devices in the chip, and the voltage swing is  $V = 0.5$  V. Therefore the total energy (in joules) in all the CMOS devices per bit of input/output data is

$$E_{\text{CMOS}} = 10^{-12} + N \left[ \log_2(10B) - \frac{1}{2} \right] \left[ 10^{-16} + 6.25d \times 10^{-11} \right] \quad B > 0.1$$

$$E_{\text{CMOS}} = 10^{-12} + N(10^{-16} + 6.25d \times 10^{-11}) \quad B \leq 0.1 \quad (3)$$

The total area  $A$  of the CMOS chip is  $d^2$  times the number of devices on the chip. Therefore,

$$A = 10NBd^2 \left[ \log_2(10B) - \frac{1}{2} \right] \quad B > 0.1$$

$$A = Nd^2 \quad B \leq 0.1 \quad (4)$$

From (3) and (4) it can be seen that the energy per bit  $E_{\text{CMOS}}$  and the chip area  $A$  are minimised with small  $d$ . However, there are two important constraints on the minimum chip size. First, to ensure that the chip does not overheat,  $A$  cannot be smaller than  $P/PD$  where  $P = BE_{\text{CMOS}} \times 10^{12}$

is the total power dissipated in the CMOS chip (excluding the O/E and E/O converters) and  $PD$  is the maximum allowable power density in a CMOS chip. Secondly, the  $10B$  O/E and  $10B$  E/O converters must be able to fit along the four edges of the chip (i.e.  $5B$  on each side). If the E/O and O/E converters are spaced by  $w$ , as shown in Fig. 3, and the chip is square, then  $A = \max(25B^2w^2, P/PD)$ . In the present analysis the maximum power density is taken to be  $PD = 100$  W/cm<sup>2</sup> [1] and the spacing  $w$  between E/O and O/E converters is 200  $\mu\text{m}$ .

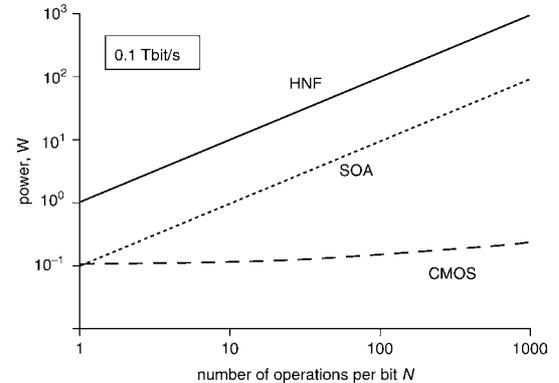


Fig. 4 Power against  $N$  at 100 Gbit/s

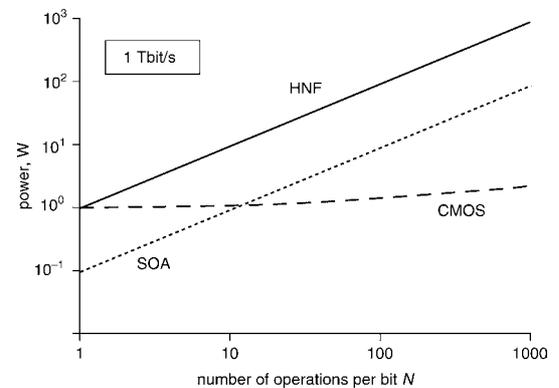


Fig. 5 Power against  $N$  at 1 Tbit/s

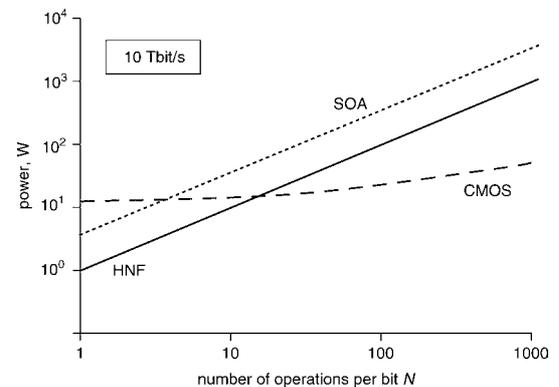


Fig. 6 Power against  $N$  at 10 Tbit/s

**Results:** Figs. 4, 5 and 6 show the power consumption against the number  $N$  of operations from input to output for each technology. Fig. 4 shows the power consumption trend for a system with  $B = 0.1$  (i.e. with a total throughput of 100 Gbit/s), Fig. 5 shows the power consumption for  $B = 1$  (a throughput of 1 Tbit/s) and Fig. 6 shows the power consumption trend for  $B = 10$  (a throughput of 10 Tbit/s). For the parameters used here, the maximum value of the CMOS device spacing  $d$  is approximately 200  $\mu\text{m}$  (for  $B = 10$  and  $N = 4$ ), and the minimum value is 6  $\mu\text{m}$  (for  $B = 1$  and 0.1, and  $N = 1000$ ). The CMOS chip area  $A$  is limited by the E/O and O/E converter spacing. This area is  $10^{-4}$  m<sup>2</sup> for  $B = 0.1$ ,  $10^{-6}$  m<sup>2</sup> for  $B = 1.0$ , and  $10^{-8}$  m<sup>2</sup> for  $B = 10$ .

For the 100 Gbit/s throughput (Fig. 4), the CMOS circuit and its associated O/E and E/O converters provide a clear power consumption advantage over the HNF and SOA circuits. For  $N = 1$ , the CMOS circuit

consumes one order of magnitude less power than the HNF fibre circuit. For  $N=1000$ , the CMOS circuit consumes 2.5 and 3.5 orders of magnitude less power than the SOA and HNF circuits, respectively.

At 1 Tbit/s (Fig. 5), the CMOS circuit consumes less power than the HNF circuit for all values of  $N$ , and less than the SOA circuit for  $N$  greater than 10. Finally, as shown in Fig. 6, the CMOS circuit consumes less power at 10 Tbit/s than the SOA and HNF circuits for  $N$  greater than 5 and 20, respectively.

*Discussion and conclusions:* The results presented here highlight the competitiveness of future generations of CMOS circuits compared with nonlinear optical devices such as highly nonlinear optical fibres and SOAs. Unlike nonlinear optical devices and circuits, CMOS circuits require O/E and E/O converters if they are to operate with optical input and output signals. However, despite the additional power consumption of the necessary O/E and E/O converters, CMOS circuits will be very competitive, even at throughputs as high as 10 Tbit/s. The only situations where CMOS does not consume less power than the all-optical devices considered here is when the number of operations per bit  $N$  is small. Therefore, barring a vast improvement in optical switching technologies, CMOS or other high-performance electronics will be the technology of choice for all but the simplest of optical signal processing.

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## References

- 1 'International Technology Roadmap for Semiconductors, 2006 Update', available: <http://public.itrs.net/>, 2006
- 2 Ching-Te, C., Bernstein, K., Joshi, R.V., Puri, R., Kim, K.E., Nowak, J., Ludwig, T., and Aller, I.: 'Scaling planar silicon devices', *IEEE Circuits Devices Mag.*, 2004, **20**, pp. 6–19
- 3 Ho, R., Mai, K.W., and Horowitz, M.A.: 'The future of wires', *Proc. IEEE*, 2001, **89**, pp. 490–504
- 4 Tucker, R.S., Eisenstein, G., and Korotky, S.K.: 'Optical time-division multiplexing for very high bit-rate transmission', *J. Lightwave Technol.*, 1988, **6**, pp. 1737–1749
- 5 Stubkjaer, K.E.: 'Semiconductor optical amplifier-based all-optical gates for high-speed optical processing', *IEEE J. Sel. Top. Quantum Electron.*, 2000, **6**, pp. 1428–1435
- 6 Langrock, C., Kumar, S., McGeehan, J.E., Willner, A.E., and Fejer, M.M.: 'All-optical signal processing using chi squared nonlinearities in guided-wave devices', *J. Lightwave Technol.*, 2006, **24**, pp. 2579–2592
- 7 Okuno, T., Nakanishi, T., Hirano, M., and Onishi, M.: 'Practical considerations for the application of highly nonlinear fibers'. Optical Fiber Communications Conf. (OFC 2007), Anaheim, CA, USA, 2007
- 8 Eggleton, B., Ta'eed, V., Baker, N., Choi, D.-Y., Finsterbusch, K., Fu, L., Lamont, M., Litler, I., Luther-Davies, B., Madden, S., Moss, D., Nguyen, H., and Shok-Sameri, M.: 'Calcogenide glass waveguides and gratings for all-optical signal conditioning'. Optical Fiber Communications Conf. (OFC 2007), Anaheim, CA, USA, 2007
- 9 Watanabe, S.: 'Optical signal processing using nonlinear fibers', *J. Opt. Fiber Commun. Rep.*, 2005, **3**, p. 1
- 10 Vlachos, K., Pleros, N., Bintjas, C., Theophilopoulos, G., and Avramopoulos, H.: 'Ultrafast time-domain technology and its application in all-optical signal processing', *J. Lightwave Technol.*, 2003, **21**, pp. 1857–1868
- 11 Ning, T.H.: 'CMOS in the new millennium'. IEEE 2000 Custom Integrated Circuits Conf., 2000
- 12 Kromer, C., Sialm, G., Berger, C., Morf, T., Schmatz, M.L., Ellinger, F., Erni, D., Bona, G.L., and Jackel, H.: 'A 100-mW  $4 \times 10$  Gb/s transceiver in 80-nm CMOS for high-density optical interconnects', *IEEE J. Solid-State Circuits*, 2005, **40**, pp. 2667–2679