Homework 4 [Due at lecture on Wed, March 1st]

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You must do this homework **alone**. Please staple multiple pages together.

1. In the von Neumann model, how does the processing unit use the Memory Address Register (MAR) and Memory Data Register (MDR) to process data values to and from memory? (2 pts)

   To read a location (A):
   1. Write the address (A) into the MAR.
   2. Send a “read” signal to the memory.
   3. Read the data from MDR.

   To write a value (X) to a location (A):
   1. Write the data (X) to the MDR.
   2. Write the address (A) into the MAR.
   3. Send a “write” signal to the memory

2. If a computer has 32-bit addressability and needs 8 bits to access a location in memory, what is the total memory size in **bytes**? Show your work for full credit. (2 pts)

   \[2^{32} \times 8 = 8192 \text{ bits} = 1024 \text{ bytes} \times (2^{10})\]

3. Consider a machine which implements an ISA in which every instruction is 32 bits long and has the following format: (3 pts)

<table>
<thead>
<tr>
<th>Opcode</th>
<th>DR</th>
<th>SR</th>
<th>IMMVAL</th>
</tr>
</thead>
</table>

   Where DR = Destination register, SR = Source Register, and IMMVAL = Immediate Value. The fields DR, SR are represented using the same number of bits.
If there are 7 bits for the opcode and 16 registers,
   a. How many unique opcodes can be represented?
   \[2^7 = 128\]
   
   b. What is the minimum number of bits required for the source register (SR) field?
   \[2^x \geq 16, \text{ solve for } x = 4\]
   
   c. If IMMVAL represents an unsigned value, what is the range of values (in decimal) that can be represented using the immediate value field?
   \[32 - (7 + 4 + 4) = 17 \text{ bits. 0 to } 2^{17} - 1 \ (131,071)\]

4. Examine the circuit below. The values of A and B feed through a decoder into a gated D-latch and change with every clock tick. A is In[1], and B is In[0]. Note that bits are numbered from zero ordering from right to left. So if In = 001, In[0] = 1, In[1] = 0 and In[2] = 0.

(7 pts)

(a) Fill out the following truth table between A, B, D, and WE.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>D</th>
<th>WE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

(b) Find the value of the “out” signal for each tick. Assume that upon initialization, out = 1.
5. Complete the truth table for the following combinatorial circuit. Note that bits are numbered from zero ordering from right to left. So if In = 001, In[0] = 1, In[1] = 0 and In[2] = 0. (4 pts)
6. (a) Each clock cycle, an input is provided to the finite state machine (FSM) below. Assuming that we start at state 00 and given an input for each tick, fill in the table to show the next state. (4 pts)
This is a corrected version that fixes some mistakes with the original. This question was not graded due to the error.

<table>
<thead>
<tr>
<th>Time</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>START</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>State</td>
<td>00</td>
<td>01</td>
<td>10</td>
<td>00</td>
<td>01</td>
<td>01</td>
<td>10</td>
<td>11</td>
<td>10</td>
</tr>
</tbody>
</table>

(b) What bit sequence(s) does this FSM recognize? Your answer should be a string of bits (ex. “01” or “1110”).
7. (2 pts)
(a) Suppose a decoder can take five inputs. How many output lines will it have?

\[ 2^5 \]

(b) A multiplexer has n input lines. How many select lines will it have?

\[ \log_2(n) \]

8. (6 pts)
(a) Describe how RS latches can be used to build gated D-latches.
RS latches are simple storage elements that can used to either hold a previous value inside a latch or to set it to 1 or 0. Gated D-latches add a write-enable element that controls whether or not the RS latch will take a new value. If \( WE = 1 \), the RS latch takes the new D value. If \( WE = 0 \), D is ignored.

(b) Describe how gated D-latches can be used to build master-slave flipflops.
Master-slave flipflops are a pair of gated d-latches that incorporate an additional clock element. When the clock is high, the D input is stored in the first latch and the second latch stays the same. Likewise, when the clock is low, the first latch's output is stored in the second latch, and the first latch does not change. The result is that output can only change state when the clock makes a transition from high to low.

(c) Describe how gated D-latches can be used to build a register.
Registers are a collection of gated D-latches that are controlled by a common WE. Each D-latch stores 1 bit, and when \( WE = 1 \), an n-bit D-value is written to the register.