Sankaralingam Panneerselvam

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Research Interests

Operating systems, Storage and Fault tolerant systems.

My research thesis is primarily focused on building systems to address challenges raised by current and future trends in processor designs in the context of heterogeneity. More recently, I have been designing testing infrastructure to test the fault tolerance capability in large scale systems.

Education

University of Wisconsin - Madison **Aug, 2009 - Aug, 2016**

Ph.D. in Computer Sciences

- Dissertation: System Design for Heterogeneous Architectures
- Advisor: Prof. Michael Swift

M.S. in Computer Sciences

- GPA: 3.813/4.0

College of Engineering, Guindy (CEG), Anna University **Aug, 2003 - May, 2007**

B.E. in Computer Science

- GPA: 8.83/10.0

Publications

Drainer: A System for Simulating and Mitigating Widespread Failures
Under Submission.

Firestorm: Operating System for Power-Constrained Architecures
Sankaralingam Panneerselvam and Michael Swift
CS-TR-2016-1837, August 2016.

Rinnegan: Efficient Resource Use in Heterogeneous Architectures
Sankaralingam Panneerselvam and Michael Swift
PACT 2016.

Bolt: Faster Reconfiguration in Operating Systems
Sankaralingam Panneerselvam, Michael Swift and Nam Sung Kim
Usenix ATC 2015.

Aerie: Flexible File-System Interfaces to Storage
Haris Volos, Sanketh Nalli, **Sankaralingam Panneerselvam**, Venkatanathan Varadarajan, Prashanth Saxena and Michael Swift
EuroSys 2014.

Storage-class Memory Needs Flexible Interfaces
Haris Volos, **Sankaralingam Panneerselvam**, Sanketh Nalli, Venkatanathan Varadarajan, Prashanth Saxena and Michael Swift
APSys 2013.

Operating Systems Should Manage Accelerators
Sankaralingam Panneerselvam and Michael Swift
HotPar 2012.

Chameleon: Operating System Support for Dynamic Processors
Sankaralingam Panneerselvam and Michael Swift
ASPLOS 2012.

Dynamic Processors Demand Dynamic Operating Systems
Sankaralingam Panneerselvam and Michael Swift
HotPar 2010.

Talks

- *Bolt: Faster Reconfiguration in Operating Systems* at Wisconsin Institute on Software-defined Datacenters in Madison (WISDoM) Workshop, Madison, WI. October 2015.
- *Rinnegan: Efficient Resource Use in Heterogeneous Architiectures* at Symantec, Mountain View, CA. June 2015.
- *Bolt: Faster Reconfiguration in Operating Systems* at Usenix ATC '15, Santa Clara, CA. June 2015.
- *Rinnegan: Efficient Resource Use in Heterogeneous Architectures* at Wisconsin SyNS '13, UW-Madison, Madison, WI. November 2013.
- *Chameleon: Operating Systems Support for Dynamic Processors* at Wisconsin Institute on Software-defined Datacenters in Madison (WISDoM) Workshop, Madison, WI. November 2012.
- *Operating Systems Should Manage Accelerators* at HotPar '12, Berkeley, CA. June 2012.
- *Chameleon: Operating Systems Support for Dynamic Processors* at ASPLOS '12, London, UK. March 2012.
- *Dynamic Processors Demand Dynamic Operating System* at HotPar '10, Berkeley, CA. June 2010.

Professional Experience

Facebook Inc., California, USA **October, 2017 - Present**
Research Scientist
I am part of the Disaster Recovery team that ensures the stability of Facebook's infrastructure even in the presence of a disaster that could completely take down one of Facebook's data center. I work on building testing infrastructure to verify the capacity provisioning of services.

Microsoft India Development Center, Hyderabad, India **June, 2007 - July, 2009**
Software Design Engineer
I was part of the WinSE group that builds and releases service packs, security patches and hotfixes for Windows Operating System. I was in the base team that owned the Kernel and HAL components, and worked on different flavours of Windows from Windows XP to Windows Server 2008.

Internships

Microsoft Research, Redmond, WA **June, 2013 - August, 2013**
Research Intern with James Larus
Designed a tool, Metis, to predict the performance benefits of using FPGA based accelerator for big data jobs running on COSMOS infrastructure. The tool analyzes the big data job logs and derive insights such as time spent in computation and IO wait time, tasks contributing to the critical path, and overall job speedup by accelerating job tasks.

Microsoft Research, Mountain View, CA **June, 2011 - August, 2011**
Research Intern with Dennis Fetterly and Vijayan Prabhakaran
Worked on improving the intermediate file access performance in Dryad. The native system creates and writes to many intermediate files resulting in lot of disk seeks. We explored a LFS based design where multiple intermediate files are written sequentially on a single log file reducing seeks greatly and improved the overall job performance.

Epic Systems, Verona, WI **Sep, 2009 - Jan, 2010**
Research Assistant
Part of EpicEarth team that works on developing a platform/framework making it easy for the medical physicians to share knowledge/information with their peers in the field.

Trilogy E-Business Software India Pvt. Ltd., Bengaluru, India **May, 2006 - July, 2006**
Software Engineering Intern
Designed and implemented Proxy Testing Framework for complete testing automation of HTML based web interface. The basic idea is to auto-generate testing scripts based on the XML based specifications written for the web page. The framework could only verify if the interface worked but it cannot verify the results returned.

Teaching Experience

CS 537: Introduction to Operating Systems **Spring 2015**
Instructor
Primary instructor for the introduction to OS course. Lectured a class of 65 students including junior/senior level undergraduates, and graduate students and also responsible for setting projects (based on Linux and xv6), and exams for the course.

Research Experience

Design of Operating Systems for Dynamic Processors
Dynamic processors can reconfigure cores at runtime by pooling resources from neighboring cores. This enables such processors to address the needs of both sequential and parallel programs. This work focus on providing better operating system support for dynamic processors. The system built faster software reconfiguration mechanism, abstraction to capture the hardware intricacies and reconfiguration-aware resource management.

Fast Reconfiguration in Operating Systems
Scaling (adding or removing) the number of cores has lot of benefits such as energy savings and virtual machine scaling. However, the latency of software reconfiguration mechanisms like hotplug are high in the order of few milliseconds. This work applies the principle of removing non-critical operations from the critical path and defering their execution to a later point in time. This helped to bring down the latency of the reconfiguration mechanism by 20x.

Efficienct Resource use in Accelerator Rich Systems
Accelerators are becoming common in processors to improve performance and power/energy efficiency. There are two major trends that make task placement harder in such architectures. First, a single task can be run on different compute units like a parallel task on CPUs or GPU. Second, contention for accelerators can arise due to sharing. This work performs task placement by analyzing the power-peformance trade-off on all compute units where the task can run.

Systems for Power-Constrained Architectures
Current processors are over-provisioned with respect to the power limit and the compute units in processors run at a conservative performance to stay within the power limit. This is done to control the heat dissipation. Though cooling devices are available, the cooling capacity can vary with device form factors and high transistor count results in more heat dissipation. This work targets to achieve power and thermal awareness in the system in allowing the right set of applications to meet their goals.

File System for Storage-Class Memory
With low-latency storage-class memory, software can be a major contributor to access latency. Aerie revists the software storage stack to evaluate its suitability for the new storage technologies. The work argues for a new file system architecture with direct access to storage for applications since the software overhead dominates data access latency from storage. The new architecture supports application specific storage interface to better exploit the storage performance.

Lost in Space
Object tagging has been primarily used in inventory management. However, tags (passive) used in such environments are not suitable for identification over large spaces. The aim of this work is to provide a cost effective and an efficient method to locate objects in physical space. Custom tags and scanners were designed based on RF technology and the sensing ranges achieved were sufficient enough for them to be deployed in house-holds or small business housings.

Professional Activities

- Shadow Program Committee member, EuroSys 2015.

Awards and Honors

- Awarded the best graduate student instructor for the academic year 2014-2015 by Department of Computer Sciences, University of Wisconsin-Madison.
- Summer Research Fellowship in 2010 from Department of Computer Sciences, University of Wisconsin-Madison.
- Travel Grants for ATC 2015, SOSP 2013, ASPLOS 2012, HotPar 2012, HotPar 2010.
- Qualified and participated in ACM Asia regional programming contest finals, Coimbatore 2006.
- Placed first in school in the state wide matriculation examination held in 2003.
- Organizer of Debugging event at Kurukshetra 2007 and Abacus 2007, national level technical symposiums hosted by College of Engineering, Guindy.

References

Prof. Michael Swift
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University of Wisconsin, Madison.
Email: swift@cs.wisc.edu

Prof. David Wood
Professor, Department of Computer Sciences
University of Wisconsin, Madison.
Email: david@cs.wisc.edu

Prof. Nam Sung Kim
Associate Professor, Department of Computer Sciences
University of Illinois, Urbana-Champaign.
Email: nskim@illinois.edu