Hello!

CONCURRENCY: INTRODUCTION

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ADMINISTRIVIA

- Project 3 done?!

- Code review: Sign up?

- Midterm I details: Piazza

Survey

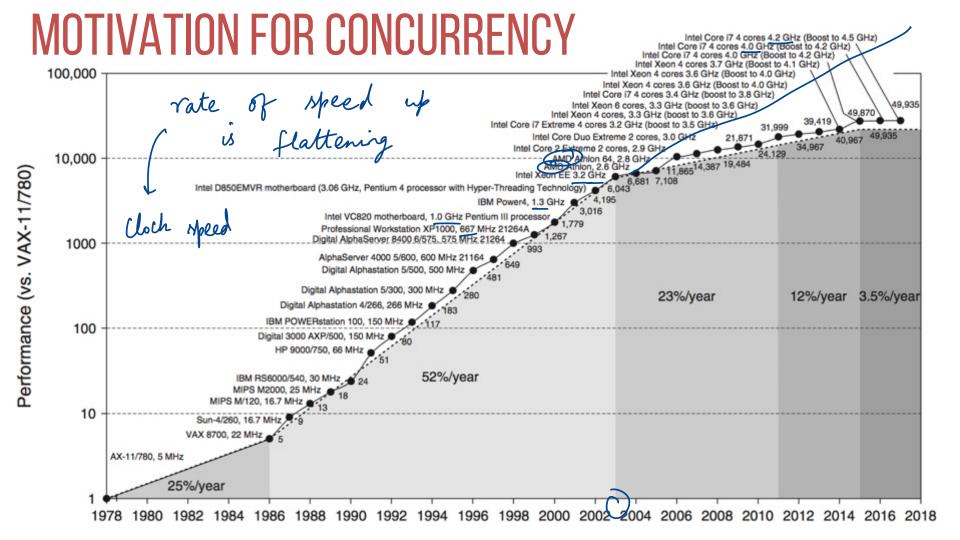
AGENDA / LEARNING OUTCOMES

Concurrency

What is the motivation for concurrent execution?

What are some of the challenges?

CONCURRENCY



MOTIVATION

CPU Trend: Same speed, but multiple cores

Goal: Write applications that fully utilize many cores

Option 1: Build apps from many communicating processes

- Example: Chrome (process per tab)
- Communicate via pipe() or similar

4 processes

Pros?

Don't need new abstractions; good for security

Lore

Core

Cons?

- Cumbersome programming
- High communication overheads
- Expensive context switching (why expensive?)

Is | grep wish

spipe operator

CONCURRENCY: OPTION 2

New abstraction: thread

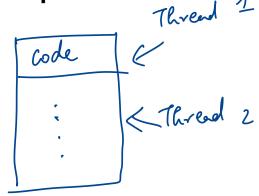
Threads are like processes, except:

instructions { } instructions

simultaneously

multiple threads of same process share an address space

Divide large task across several cooperative threads Communicate through shared address space



COMMON PROGRAMMING MODELS

printing

Multi-threaded programs tend to be structured as:

Producing deta

Producer/consumer

Multiple producer threads create data (or work) that is handled by one of the multiple consumer threads

Pipeline

Task is divided into series of subtasks, each of which is handled in series by a different thread

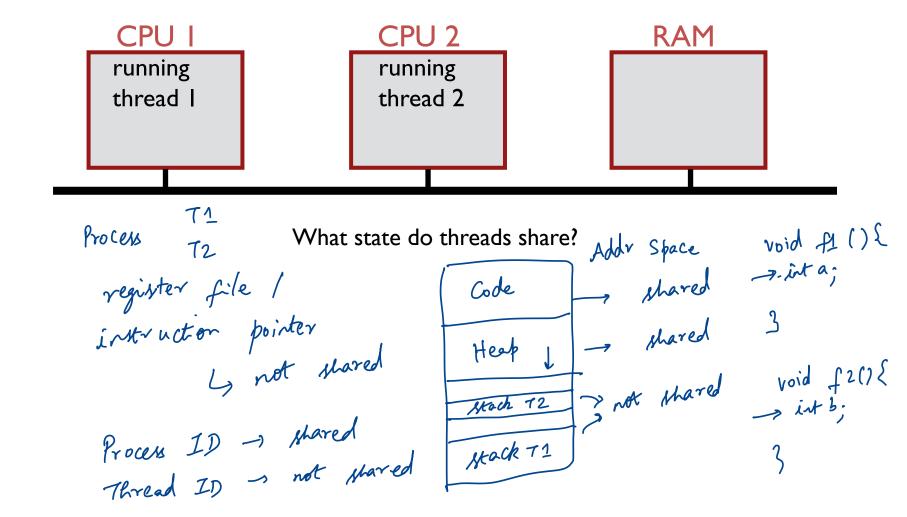
Defer work with background thread

One thread performs non-critical work in the background (when CPU idle)

text editor
Ly back ground linteractive
auto save I spell the thing

deta

- rem



THREAD VS. PROCESS

Multiple threads within a single process share:

- Process ID (PID)
- Address space: Code (instructions), Most data (heap)
- Open file descriptors → stdout, stder
- Current working directory
- User and group id

Each thread has its own

- Thread ID (TID)
- Set of registers, including Program counter and Stack pointer
- Stack for local variables and return addresses (in same address space)

OS SUPPORT: APPROACH 1

User-level threads: Many-to-one thread mapping

- Implemented by user-level runtime libraries Create, schedule, synchronize threads at user-level
- OS is not aware of user-level threads OS thinks each process contains only a single thread of control

Advantages

- Does not require OS support; Portable
- Lower overhead thread operations since no system call

Disadvantages?

- Cannot leverage multiprocessors scheduler only runs
 Entire process blocks when one thread blocks 1/2 speration BLOCKED arise grows

OS SUPPORT: APPROACH 2

reate preads Areads OS 133 process 1

Process 1

Kernel-level threads: One-to-one thread mapping

- OS provides each user-level thread with a kernel thread
- Each kernel thread scheduled independently
- Thread operations (creation, scheduling, synchronization) performed by OS

Advantages

- Each kernel-level thread can run in parallel on a multiprocessor
- When one thread blocks, other threads from process can be scheduled

Disadvantages

- Higher overhead for thread operations
- OS must scale well with increasing number of threads

THREAD SCHEDULE

creates thread

volatile int balance = 0; }, coole int loops; — segment int main(int argc, char *argv[]) { loops = atoi(argv[1]); pthread t p1, p2; printf("Initial value : %d\n", balance); warts void *worker(void *arg) { P2 starts Pthread_create(&p1, NULL, worker, NULL); int i: Pthread_create(&p2, NULL, worker, NULL); Pthread join(p1, NULL); for (i = 0; i < loops; i++) { balance++; ____, increment printf("Final value : %d\n", balance);
thread_exit(NULL);

Pthread_join(p2, NULL);
printf("Final value : %d\n", balance);
return 0; pthread_exit(NULL); mitial value: 0

Tinal value: 162901

Expert 200,000

THREAD SCHEDULE #1

```
balance = balance + 1;
 balance at 0x9000
                                                       Thread I
                                                                            Thread 2
                                          thread
 State:
                                                                         %eax:
                                                     %eax:
                                         control
 0x9000: 100
                                                     %rip:
                                                                          %rip:
 %eax:
                                          blocks:
 %rip = 0x195
                                       read balance register

add 1 register

write register balance
√0x195 mov 0x9000, %eáx
 0x19a add $0x1, %eax
 0x19d
         mov %eax, 0x9000
                                                                              write
    diff
interleaving can
lead to diff results
```

THREAD SCHEDULE #2

```
balance = balance + 1;
balance at 0x9cd4
```

State:

0x9000: 100

%eax:

%rip = 0x195

0x195 mov 0x9000, %eax

0x19a add \$0x1, %eax

0x19d mov %eax, 0x9000

thread control blocks:





nemory

TIMELINE VIEW

balance (x) 13

Thread I

mov 0×123 , %eax

add %0x1, %eax

mov %eax, 0x123 1 1

Thread 2

mov 0x123, %eax

add %0x2, %eax

3 mov %eax, 0x123

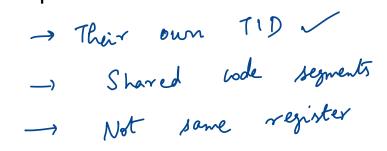
added 3 to granted variable

QUIZ 9

https://tinyurl.com/cs537-fa24-q9

Process A with threads TAI and TA2 and process B with a thread TBI.

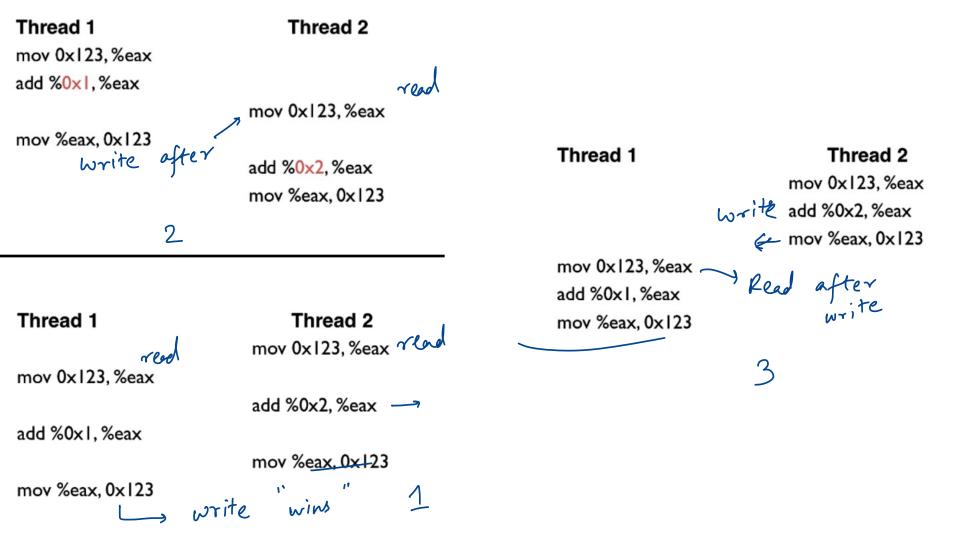
I. With respect to TAI and TA2 which of the following are true?



2. Which of the following are true with respect to TA1 and TB1?

→ False





NON-DETERMINISM

Concurrency leads to non-deterministic results

- Different results even with same inputs
- -"race conditions"

Whether bug manifests depends on CPU schedule!

How to program: imagine scheduler is malicious?!

Ly any thread scheduler

WHAT DO WE WANT?

Want 3 instructions to execute as an uninterruptable group That is, we want them to be atomic

More general: Need mutual exclusion for critical sections if thread A is in critical section C, thread B isn't (okay if other threads do unrelated work)

SYNCHRONIZATION

Build higher-level synchronization primitives in OS

Operations that ensure correct ordering of instructions across threads

Use help from hardware

Motivation: Build them once and get them right

Monitors
Locks
Condition Variables

How do
we implement
Test&Set
Stores
Disable Interrupts

LOCKS

LOCKS

Lock 11 T1 cacquire

Goal: Provide mutual exclusion (mutex)

Allocate and Initialize

- Pthread mutex t mylock = PTHREAD_MUTEX_INITIALIZER;

Acquire

b →

threa

2 (Cess

same

Acquire exclusion access to lock;

- tion)
- Wait if lock is not available (some other process in critical section)
- Spin or block (relinquish CPU) while waiting
- Pthread mutex lock(&mylock);

Release

- Release exclusive access to lock; let another process enter critical section
- Pthread_mutex_unlock(&mylock);

LOCK IMPLEMENTATION GOALS

Correctness

- Mutual exclusion
 Only one thread in critical section at a time
- Progress (deadlock-free)
 If several simultaneous requests, must allow one to proceed
- Bounded (starvation-free)
 Must eventually allow each waiting thread to enter

Fairness: Each thread waits for same amount of time

Performance: CPU is not used unnecessarily

IMPLEMENTING SYNCHRONIZATION

Atomic operation: No other instructions can be interleaved

Approaches

- Disable interrupts
- Locks using loads/stores
- Using special hardware instructions

IMPLEMENTING LOCKS: W/INTERRUPTS

Turn off interrupts for critical sections

- Prevent dispatcher from running another thread
- Code between interrupts executes atomically

```
void acquire(lockT *1) {
    disableInterrupts();
}
void release(lockT *1) {
    enableInterrupts();
}
```

Disadvantages?

Only works on uniprocessors

Process can keep control of CPU for arbitrary length

Cannot perform other necessary work

IMPLEMENTING LOCKS: W/LOAD+STORE

Code uses a single **shared** lock variable

```
// shared variable
boolean lock = false;
void acquire(Boolean *lock) {
    while (*lock) /* wait */;
    *lock = true;
}
void release(Boolean *lock) {
    *lock = false;
}
```

Does this work? What situation can cause this to not work?

RACE CONDITION WITH LOAD AND STORE

Both threads grab lock!

Problem: Testing lock and setting lock are not atomic

XCHG: ATOMIC EXCHANGE OR TEST-AND-SET

How do we solve this? Get help from the hardware!

```
// xchg(int *addr, int newval)
// return what was pointed to by addr
// at the same time, store newval into addr
int xchg(int *addr, int newval) {
  int old = *addr;
  *addr = newval;
  return old;
}

movl 4(%esp), %edx
movl 8(%esp), %eax
xchgl (%edx), %eax
ret
```

LOCK IMPLEMENTATION WITH XCHG

int xchg(int *addr, int newval)

```
typedef struct lock t {
   int flag;
} lock t;
void init(lock t *lock) {
    lock -> flaq = ??;
void acquire(lock t *lock) {
   ????;
   // spin-wait (do nothing)
void release(lock t *lock) {
    lock -> flag = ??;
```

OTHER ATOMIC HW INSTRUCTIONS

```
int CompareAndSwap(int *addr, int expected, int new) {
 int actual = *addr;
 if (actual == expected)
    *addr = new;
 return actual;
void acquire(lock t *lock) {
    while(CompareAndSwap(&lock->flag, , ) == );
    // spin-wait (do nothing)
```

NEXT STEPS

Midterm I: Next week

Next class: More about locks!