

CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

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Examination 4

In Class (50 minutes)

Wednesday, Dec 14, 2011

Weight: 17.5%

NO: BOOK(S), NOTE(S), CALCULATORS OF ANY SORT.

This exam has 12 pages, including a blank page at the end. Plan your time carefully, since some problems are longer than others. You must turn in pages 1 to 9.

LAST NAME: _____

FIRST NAME: _____

SECTION: _____

ID# _____

Question	Maximum Point	Points
1	3	
2	5	
3	4	
4	3	
5	5	
6	5	
7	5	
Total	30	

Q1. Syntax Errors in LC-3 Assembly Code (3 points)

a. Circle any illegal labels in an assembly language programs: **(1 point)**

- ADD
- END
- .FILL
- BLKW
- OR
- NAND

b. The following program has multiple syntax errors. One of them, along with an explanation of the error, is indicated in the table below. In the two blank rows of the table, identify and explain two more syntax errors. **(2 points)**

```

                .ORIG x3000
                LDI     R1, COUNT
                AND     R1, R1, M1
LOOP           LEA     R0, x2FF
                ADD     R0, R1, R2
                BRZ     LOOP
                NOT     R1, R1, R1
                HALT
M1             .FILL   x4000
COUNT        .FILL   #100
                .END
    
```

Instruction	Error
AND R1, R1, M1	Can't use a label as operand

Q2. Two-Pass Assembly Process (5 points)

An assembly language LC-3 program is given below:

```

        .ORIG      x3000
L1      LEA        R1, L1
        AND        R2, R2, x0
        ADD        R2, R2, x3
        LD         R3, P1
L2      LDR        R0, R1, xC
        TRAP       x21          ; OUT (Write char)
        ADD        R3, R3, #-1
        BRz        GLUE
        ADD        R1, R1, R2
        BRnzp     L2
GLUE    HALT
P1      .FILL      x7
        .STRINGZ   "GWHoeiolTdchboeymreee"
        .END
    
```

- a. Fill in the symbol table created by the first pass of the assembler on the above program. **(2 points)**

Symbol Name	Address
L1	
L2	
GLUE	
P1	

- b. After the program is assembled and loaded, what binary pattern is stored in memory location x3005? **(1 point)**

- c. What is the output of this program? **(2 points)**

Q3. Logical Error (4 points)

We want the following code to shift the value at memory location M1 to the left by the number of bits stored at memory location M2, but there is **one** error in this code.

```
        .ORIG      x3000

        LD         R1, M1
        LD         R2, M2

LOOP    BRz        DONE
        ADD        R2, R2, #-1
        ADD        R1, R1, R1
        BRnzp     LOOP
DONE    HALT

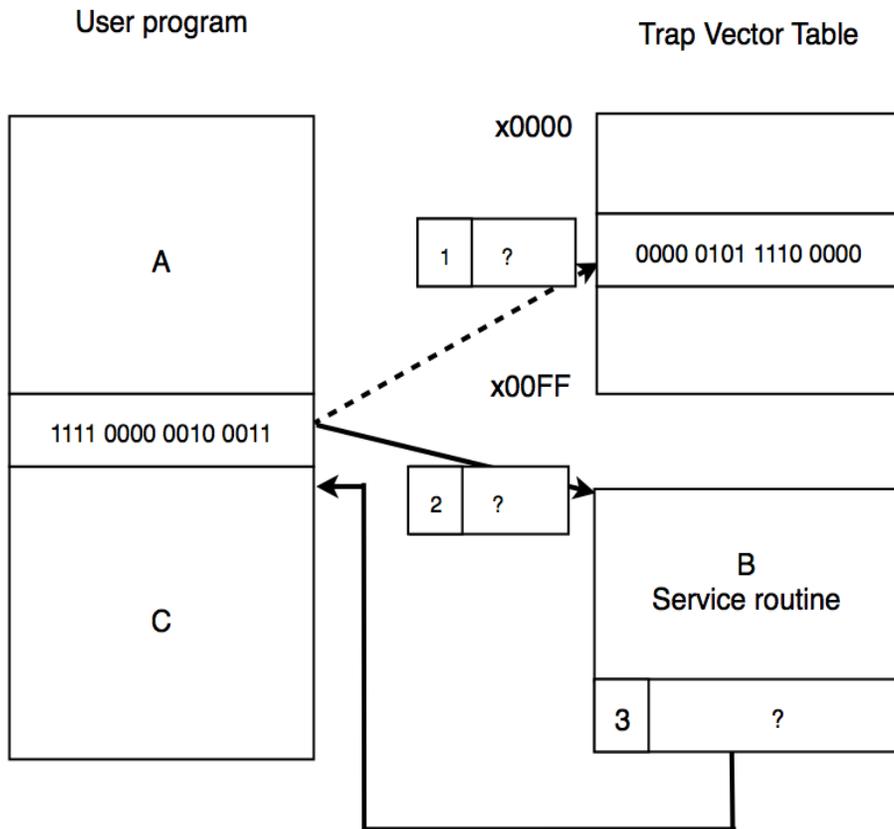
M1      .FILL     x000C
M2      .FILL     x0004
        .END
```

a. How many times does the instruction labeled LOOP get executed? Explain. **(2 points)**

b. What is wrong with this program? Explain. **(2 points)**

Q4. Trap Handling(3 points)

The figure shown below represents the flow control from a user program to an OS service routine and back when a trap instruction is called. The flow control goes from A within a user program, to B the operating system service routine, back to the user program C. Fill out the the three empty boxes below corresponding with question marks. Boxes 1 and 2 should be filled with addresses and box 3 should be filled with an instruction.



Write your answers in **hexadecimal**.

1	2	3

Q5. Traps and subroutines (5 points)

An LC-3 programmer wrote the code below to read 10 single digit decimal number from the keyboard, compute their average, and display the ceiling of the resultant average on the monitor.

Fill in the blanks below with assembly code to complete the program.

```

                .ORIG      x3000

                AND       R2, R2, #0           ; R2 keeps track of the sum
                LD        R6, CHtoD           ; Char->Digit template
                LD        R5, DtoCH           ; Digit->Char template
                LD        R7, COUNT           ; Initialize to 10
                ST        __, SAVEDREG         ; Save ?? upon call of trap
AGAIN          TRAP      x23                 ; Get char
                LD        _____          ; Restore ?? before continuing
                ADD       R0, R0, R6         ; Convert to number
                ADD       R2, R2, R0         ; Add the new number to the sum
                ADD       R7, R7, -1        ; Decr counter
                ST        __, SAVEDREG         ;
                BRp      AGAIN              ; More digit?
                LD        R1, COUNT          ;

                _____                  ;
                ADD       R0, R0, R5         ; Convert to char
                TRAP      x21               ; Output char
                HALT

; DIV subroutine
; Args: R2,R1  RET: R0=R2/R1
DIV           AND       R0, R0, #0           ; Initialize to 0
                NOT      R1, R1             ;
                ADD      R1, R1, #1         ; Negate R1
LOOPDIV      ADD       R0, R0, #1
                _____                  ;
                BRP      LOOPDIV
                RET

DtoCH        .FILL     x0030
CHtoD        .FILL     xFFD0
COUNT       .FILL     #10

SAVEDREG     .BLKW     1

                .END
```


Q7. General Questions (5 points, 1 point each)

Circle the **best** answer for the following questions about LC-3:

1. Which of the following can be used only once per file?
 - a. .STRINGZ
 - b. .BLKW
 - c. .ORIG
 - d. .FILL

2. Which of the following is true about “callee-save”?
 - a. Used by calling routine to save and restore registers that will be used in the routine
 - b. Save R7 before calling TRAP
 - c. Save R0 before calling TRAP x23
 - d. Used by called routine to save registers used by the routine

3. Suppose `JSR label` is stored at memory location x3000. After the instruction is executed, which of the following is true if `label=x3050` and `R7=x4000` before execution?
 - a. `R7 = x3050`
 - b. `R7 = x3001`
 - c. `R7 = x3000`
 - d. `R7 = x4000`

4. Which bit in the KBSR is the interrupt enable bit?
 - a. 15
 - b. 14
 - c. 13
 - d. 12

5. Which of the following is **not true** about interrupt driven I/O?
 - a. The device controls the interaction by sending a special signal to the processor when it is ready
 - b. It is more efficient than polling
 - c. It has built in priority levels for different device requests
 - d. The processor must routinely check the status register for the device until new data arrives or the device is ready

Scratch Page

ASCII Table

<i>Character</i>	<i>Hex</i>	<i>Character</i>	<i>Hex</i>	<i>Character</i>	<i>Hex</i>	<i>Character</i>	<i>Hex</i>
nul	00	sp	20	Ⓐ	40	`	60
soh	01	!	21	A	41	a	61
stx	02	"	22	B	42	b	62
etx	03	#	23	C	43	c	63
eot	04	\$	24	D	44	d	64
enq	05	%	25	E	45	e	65
ack	06	&	26	F	46	f	66
bel	07	'	27	G	47	g	67
bs	08	(28	H	48	h	68
ht	09)	29	I	49	i	69
lf	0A	*	2A	J	4A	j	6A
vt	0B	+	2B	K	4B	k	6B
ff	0C	,	2C	L	4C	l	6C
cr	0D	-	2D	M	4D	m	6D
so	0E	.	2E	N	4E	n	6E
si	0F	/	2F	O	4F	o	6F
dle	10	0	30	P	50	p	70
dc1	11	1	31	Q	51	q	71
dc2	12	2	32	R	52	r	72
dc3	13	3	33	S	53	s	73
dc4	14	4	34	T	54	t	74
nak	15	5	35	U	55	u	75
syn	16	6	36	V	56	v	76
etb	17	7	37	W	57	w	77
can	18	8	38	X	58	x	78
em	19	9	39	Y	59	y	79
sub	1A	:	3A	Z	5A	z	7A
esc	1B	;	3B	[5B	{	7B
fs	1C	<	3C	\	5C		7C
gs	1D	=	3D]	5D	}	7D
rs	1E	>	3E	^	5E	~	7E
us	1F	?	3F	_	5F	del	7F

LC-3 Instruction Set (Entered by Mark D. Hill on 03/14/2007; last update 03/15/2007)

PC': incremented PC. setcc(): set condition codes N, Z, and P. mem[A]:memory contents at address A.
 SEXT(immediate): sign-extend immediate to 16 bits. ZEXT(immediate): zero-extend immediate to 16 bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	0	0	1		DR		SR1		0	0	0		SR2				ADD DR, SR1, SR2 ; Addition			
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
DR SR1 + SR2 also setcc()																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	0	0	1		DR		SR1		1		imm5						ADD DR, SR1, imm5 ; Addition with Immediate			
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
DR SR1 + SEXT(imm5) also setcc()																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	1	0	1		DR		SR1		0	0	0		SR2				AND DR, SR1, SR2 ; Bit-wise AND			
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
DR SR1 AND SR2 also setcc()																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	1	0	1		DR		SR1		1		imm5						AND DR,SR1,imm5 ; Bit-wise AND with Immediate			
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
DR SR1 AND SEXT(imm5) also setcc()																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	0	0	0		n		z		p		PCoffset9						BRx,label (where x={n,z,p,zp,np,nz,nzp}); Branch			
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
GO ((n and N) OR (z AND Z) OR (p AND P))																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
if(GO is true) then PCPC' + SEXT(PCoffset9)																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
1	1	0	0		0	0	0		BaseR		0	0	0	0	0	0		JMP BaseR ; Jump		
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
PC BaseR																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	1	0	0		1		PCoffset11						JSR label ; Jump to Subroutine							
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
R7 PC', PC PC' + SEXT(PCoffset11)																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	1	0	0		0	0	0		BaseR		0	0	0	0	0	0		JSRR BaseR ; Jump to Subroutine in Register		
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
temp PC', PC BaseR, R7 temp																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	0	1	0		DR		PCoffset9						LD DR, label ; Load PC-Relative							
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
DR mem[PC' + SEXT(PCoffset9)] also setcc()																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
1	0	1	0		DR		PCoffset9						LDI DR, label ; Load Indirect							
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
DRmem[mem[PC'+SEXT(PCoffset9)]] also setcc()																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	1	1	0		DR		BaseR		offset6						LDR DR, BaseR, offset6 ; Load Base+Offset					
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
DR mem[BaseR + SEXT(offset6)] also setcc()																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
1	1	1	0		DR		PCoffset9						LEA, DR, label ; Load Effective Address							
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
DR PC' + SEXT(PCoffset9) also setcc()																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
1	0	0	1		DR		SR		1	1	1	1	1	1		NOT DR, SR ; Bit-wise Complement				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
DR NOT(SR) also setcc()																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
1	1	0	0		0	0	0		1	1	1	0	0	0	0	0		RET ; Return from Subroutine		
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
PC R7																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
1	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0		RTI ; Return from Interrupt		
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
See textbook (2nd Ed. page 537).																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	0	1	1		SR		PCoffset9						ST SR, label ; Store PC-Relative							
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
mem[PC' + SEXT(PCoffset9)] SR																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
1	0	1	1		SR		PCoffset9						STI, SR, label ; Store Indirect							
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
mem[mem[PC' + SEXT(PCoffset9)]] SR																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
0	1	1	1		SR		BaseR		offset6						STR SR, BaseR, offset6 ; Store Base+Offset					
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
mem[BaseR + SEXT(offset6)] SR																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
1	1	1	1		0	0	0	0		trapvect8						TRAP ; System Call				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
R7 PC', PC mem[ZEXT(trapvect8)]																				
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
1	1	0	1														; Unused Opcode			
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----																				
Initiate illegal opcode exception																				