CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

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Midterm Examination 2

In Class (50 minutes)

Friday, October 24, 2014

Weight: 17.5%

NO: BOOK(S), NOTE(S), OR CALCULATORS OF ANY SORT.

The exam has **nine** pages. **Circle your final answers**. Plan your time carefully since some problems are longer than others. You **must turn in the pages 1-9**. Use the blank sides of the exam for scratch work.

LAST NAME: ____

FIRST NAME: ____

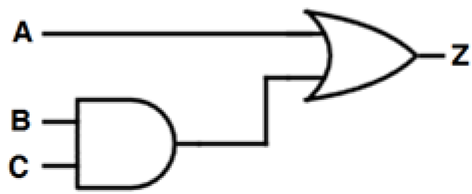
ID#: ____

Problem	**Maximum Points**	**Points Earned**
1	4	
2	6	
3	3	
4	5	
5	3	
6	9	
Total	30	

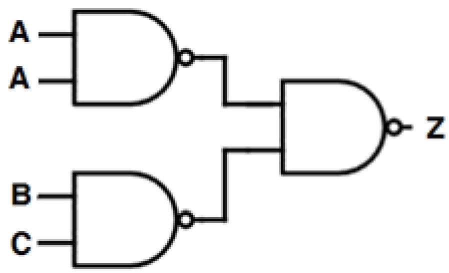
Problem 1 **(4 Points)**

Consider the logic equation Z = A OR (C AND B).

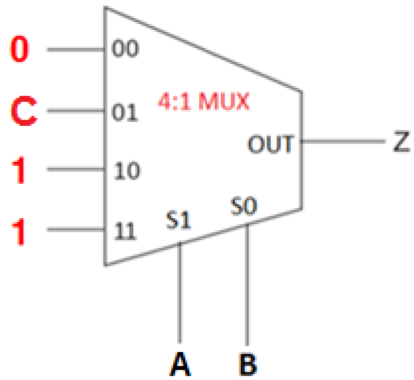
a. **(1 point)** Draw a **gate-level** circuit for Z using NOT gates and 2-input AND/OR gates.



b. **(1 points)** Draw a **gate-level** circuit for Z using only 2-input NAND gates.

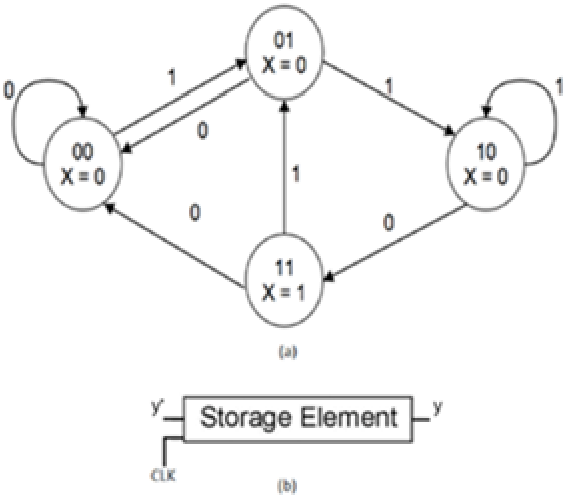


c. **(2 points)** Implement a logic circuit for Z using a 4x1 multiplexer where A and B are connected to the select lines. Draw your answer using the 4x1 multiplexer below. **Do not use any additional logic gates**.



Problem 2 **(6 Points)**

The finite state machine (FSM) below (in Figure 1(a)) recognizes a certain bit sequence. The machine takes one input every clock cycle, which can be 1 or 0. The machine outputs a ‘1’ when this certain bit sequence is recognized; otherwise it outputs a ‘0’. Each state is represented as S_1S_0. For example, the state marked as “01” has $S_1 = 0$, and $S_0 = 1$. X is the output in each state. $S_1'S_0'$ represents the next state and the labels on each transition is the input value that triggers the transition. Assume that the initial state is 00.

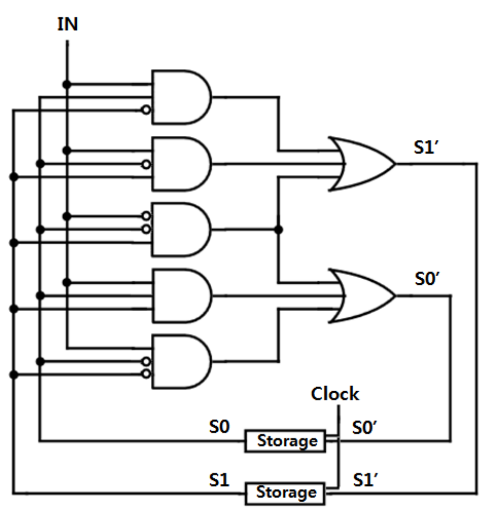


S1	SO	IN	S1'	SO'
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	0	1

Figure 1

a. **(2 points)** Complete the Next State truth table for the FSM.

b. **(3 Points)** Draw the logic circuit which implements the above FSM using combinational logic and flip flops. Use representation shown in figure 1(b) for any 1-bit flip flop required in the circuit (where CLK is the clock). You can use any kind of logic gates for implementing the combinational logic. Note: You should implement both the states (S1, S0) as well as the output (X).



c. **(1 point)** Which bit sequence does the above FSM recognize? Your answer should be a string of bits (e.g, “1001” or “11001”).

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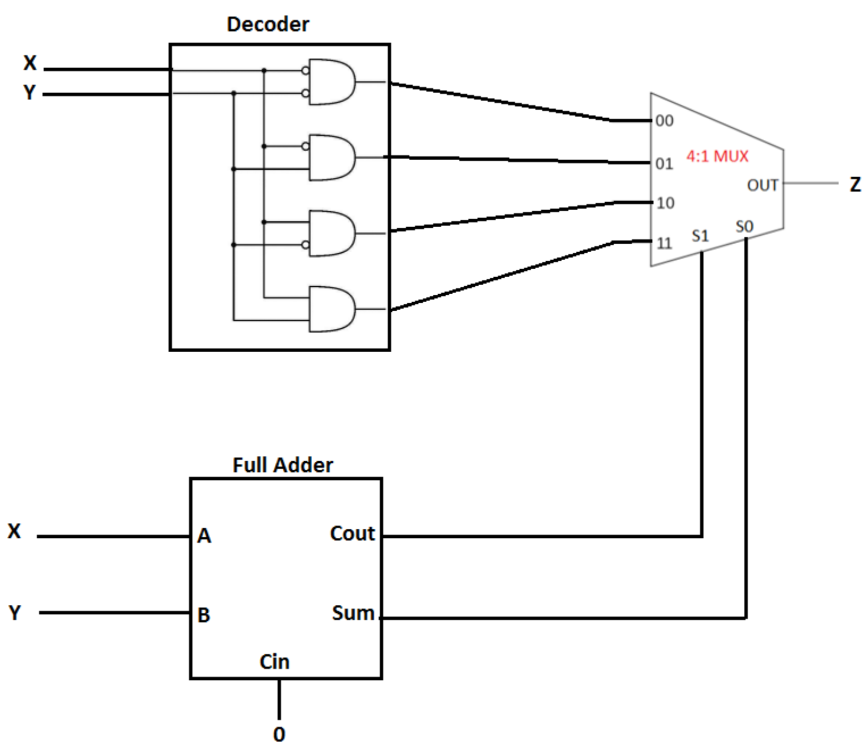
Problem 3 **(3 Points)**

Consider the following circuit containing a multiplexer, a single-bit full adder and a decoder. X and Y are inputs to this circuit, and the circuit produces an output Z. Fill in the truth table below for this combinational circuit.



X	Y	Z
0	0	1
0	1	1
1	0	0
1	1	0

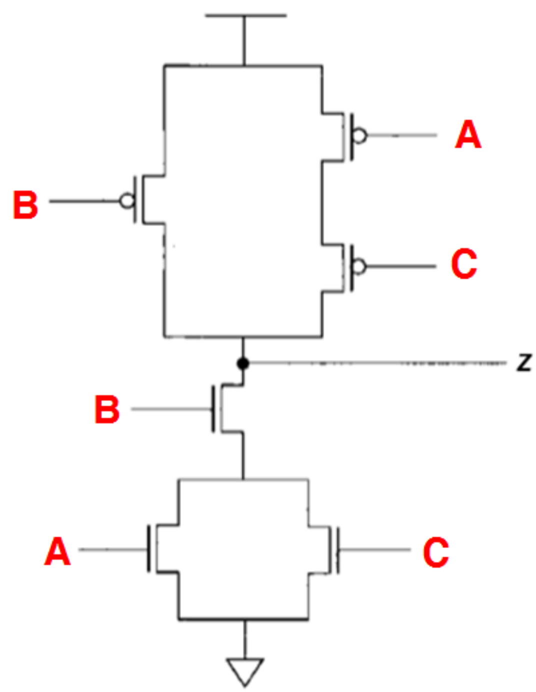
Problem 4 **(5 Points)**

Consider the logic equation Z = NOT(B AND NOT(NOT(C) AND NOT(A))). (Hint: You may want to use DeMorgan's law to simplify the equation.)

a. **(2 points)** Fill out the following truth table for Z.

A	B	C	Z
0	0	0	**1**
0	0	1	**1**
0	1	0	**1**
0	1	1	**0**
1	0	0	**1**
1	0	1	**1**
1	1	0	**0**
1	1	1	**0**

b. **(3 points)** Label the inputs on the transistor-level circuit below so that the circuit implements the logic function Z.



Problem 5 **(3 Points)**

Suppose a 32-bit instruction takes the following format:

OPCODE	SR	DR	UNUSED	IMM

Where SR = source register, DR= destination register, IMM = immediate value

Assuming that there are 300 opcodes and the IMM field is 11-bits wide, answer the following:

a. **(1 point)** What is the minimum number of bits required to represent the OPCODE?

$\mathbf{2^9 = 512 > 300, \text{ so } 9 \text{ bits}}$

b. **(1 point)** If the source register (SR) and destination register (DR) each have 5 bits, what is the maximum number of registers supported by this instruction set architecture?

$\mathbf{2^5 = 32 \text{ registers}}$

c. **(1 point)** If the UNUSED bits were instead used for the register fields (SR and DR), how many more registers could we have in our computer?

32 – 9 – 5 – 5 – 11 = 2 bits in the UNUSED field. This means we can give 2/2 =1 bit to each the SR and DR field. So, we could represent $2^6 - 2^5 = 32$ more registers

Problem 6 **(9 Points)**

a. **(1 point)** Mention two important things that happen during the FETCH phase of the instruction cycle.

Increment PC
Read the instruction, store in IR

b. **(2 points)** How many different n-input Boolean functions are possible? Show your work.

Given n inputs, 2^{2^n} functions are possible.

c. **(1 point)** How many select lines does an n-input mux have?

Let $n = 2^y$, since we know n must be a power of 2.
The number of select lines is y, or $\log_2 n$.

>> $\log_2 n$

d. **(1 point)** How many outputs does an n-input decoder have?

A decoder has n inputs and 2^n outputs

e. **(1 point)** What is the addressability (number of bytes per memory location) of a 1024 byte memory which uses 10 bits for each memory address? Show your work.

$$\mathbf{1024\ bytes} = \mathbf{2^{10}} = \mathbf{2^{10} \times 2^{3}\ bits}$$
$$\mathbf{2^{13}\ bits} \div \mathbf{2^{10} bits} = \mathbf{2^{3}\ bits} = \mathbf{8\ bits}$$

f. **(2 points)** How many n-type transistors are present in a 32-bit wide register? Show your work.

Each Gated D latch has 4 NAND gates and 1 inverter. Each NAND gate has 2 n-type transistors, and each inverter has 1 n-type transistor.

Therefore, we have 32*4*2 + 32 = 288 n-type transistors.

g. **(1 Point)** Which of the following stages of instruction processing are required for the processing of an ADD instruction which reads value of 2 registers and stores the final value into another register. Circle all that apply:

Fetch
Decode
Evaluate address
Fetch operands from the memory
Execute Operation
Store result