CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

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Midterm Examination 2

In Class (50 minutes)

Wednesday, March13, 2013

Weight: 17.5%

NO: BOOK(S), NOTE(S), OR CALCULATORS OF ANY SORT.

The exam has 9 pages. **Circle your final answers**. Plan your time carefully since some problems are longer than others. You **must turn in the pages 1-8**.

LAST NAME: _____

FIRST NAME: _____

ID# _____

Problem	Maximum Points	Points Earned
1	6	
2	2	
3	2	
4	6	
5	2	
6	2	
7	2	
8	4	
9	4	
Total	30	

Problem 1 **(6 Points)**

For the following questions, select the **best** answer. Choose only **one answer per question**.

i. Which of the following is **not** true about a decoder?
   a. Two outputs of a decoder cannot be high at the same time.
   b. It acts like a MUX that has been connected in reverse.
   c. At least one output is high for any combination of inputs.
   d. It has more output lines than input lines.

ii. Which of the following is true about the FETCH OPERANDS phase of the instruction cycle?
   a. Reads data from register files.
   b. Loads data from memory.
   c. Both (a) and (b).
   d. None of the above.

iii. In which phase of the instruction cycle is the PC incremented?
   a. DECODE
   b. FETCH
   c. EXECUTE
   d. STORE RESULT

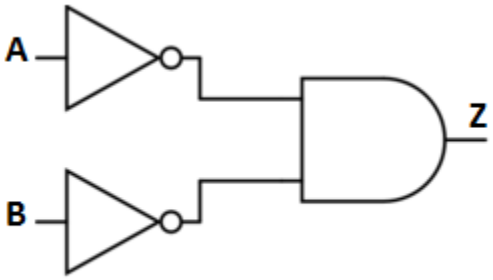
iv. How many instructions are executed per second by a machine which has a clock frequency of 40MHz and takes 10 cycles to execute an instruction?
   a. 0.10
   b. 0.25
   c. 4,000,000
   d. 1,000,000

v. Which of the following is **not** true about an instruction?
   a. Its format is specified in the Instruction Set Architecture (ISA).
   b. Specifies an operation which is executed completely or not at all.
   c. Specifies the opcode and operands to be used in its execution.
   d. Looks different from data in its representation.

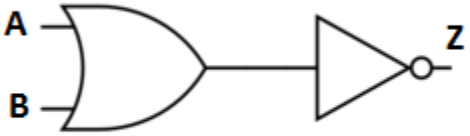
vi. How many D-latches do we need to build a memory with an addressability of 4 bits and an address space of 512 locations?
   a. 256
   b. 1024
   c. 2048
   d. 4096

Problem 2 **(2 Points)**

Are the following two combinational circuits **(a)** and **(b)** equivalent? Why or why not?



(a)

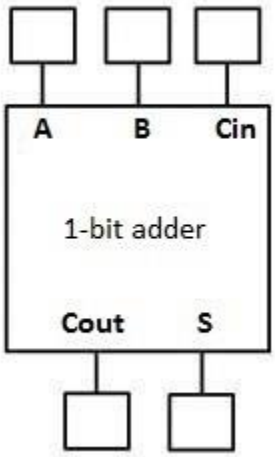


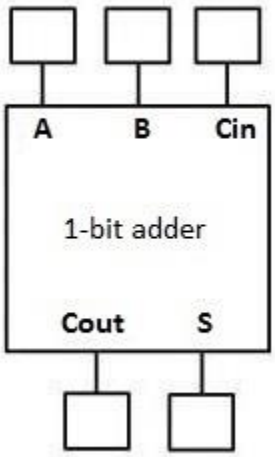
(b)

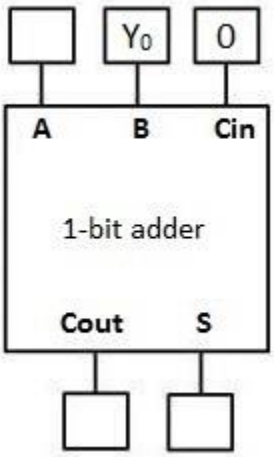
Problem 3 **(2 Points)**

Build a 3-bit adder from three 1-bit adders. The 3-bit inputs are $X_2X_1X_0$ and $Y_2Y_1Y_0$ and the 3-bit output is $Z_2Z_1Z_0$. Assume X_0, Y_0, Z_0 are the least significant bits and X_2, Y_2, Z_2 are the most significant bits. Fill the boxes in the figure below with the appropriate variable names ***and make connections if and when required***. Y_0 is filled in as an example.

Note: In each 1-bit adder, A and B are the inputs, C_{in} is the carry-in, C_{out} is the carry-out and S is the sum.



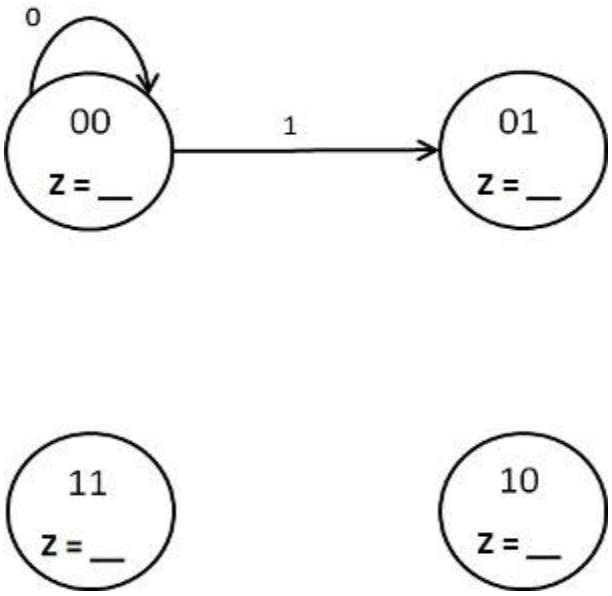




Problem 4 **(6 Points)**

Design a finite state machine (FSM) that recognizes the pattern "101" among a sequence of input bits (**IN**). When the FSM has "101" as inputs in successive bits, it should output 1. Otherwise, the output should be 0. The bits are read from left to right. For example, for the input sequence 0101101010, the FSM output should be 0001001010.

a. **Complete the state diagram below.** Each state is represented by two bits, S_1S_0. For example, the state marked as "01" has $S_1 = 0$ and $S_0 = 1$. Clearly show all possible state transitions and the output **(Z)** at each state. The transitions for the initial state "00" have been completed for you. **Assume that "11" is the state in which the sequence "101" is detected.** **(4 Points)**



b. Fill out the following **Next State truth table** for the above state diagram where $S_1'S_0'$ represents the next state. **(2 Points)**

S_1	S_0	IN	S_1'	S_0'

Problem 5 **(2 Points)**

List and describe briefly the several basic components of the von Neumann model.

Problem 6 **(2 Points)**

For the following truth table, with inputs A, B, C and output Z, draw the gate level circuit using NOT gates and 3-input AND/OR gates.

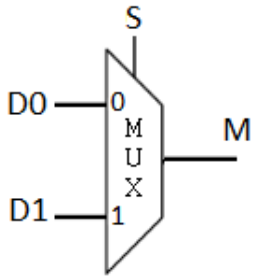
A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Problem 7 **(2 Points)**

In the von Neumann model, list the **two** interface registers involved in all memory accesses and describe the purpose of each of them.

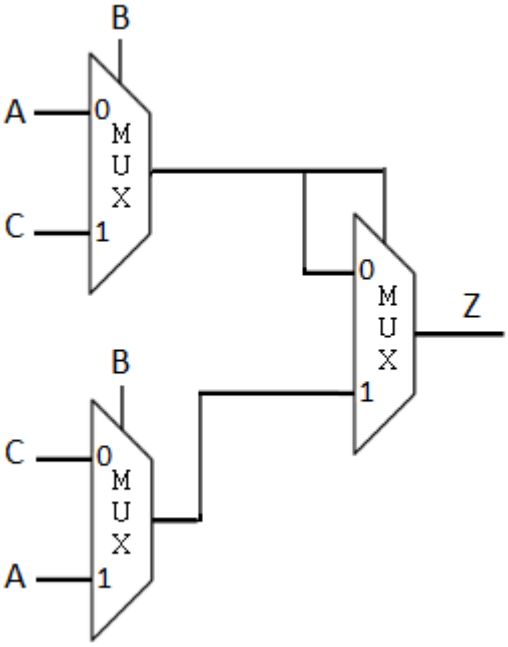
Problem 8 **(4 Points)**

Suppose the following is used to represent a 2:1 multiplexer:



Where **S** is the select line, **D0** and **D1** are the inputs and **M** is the output.

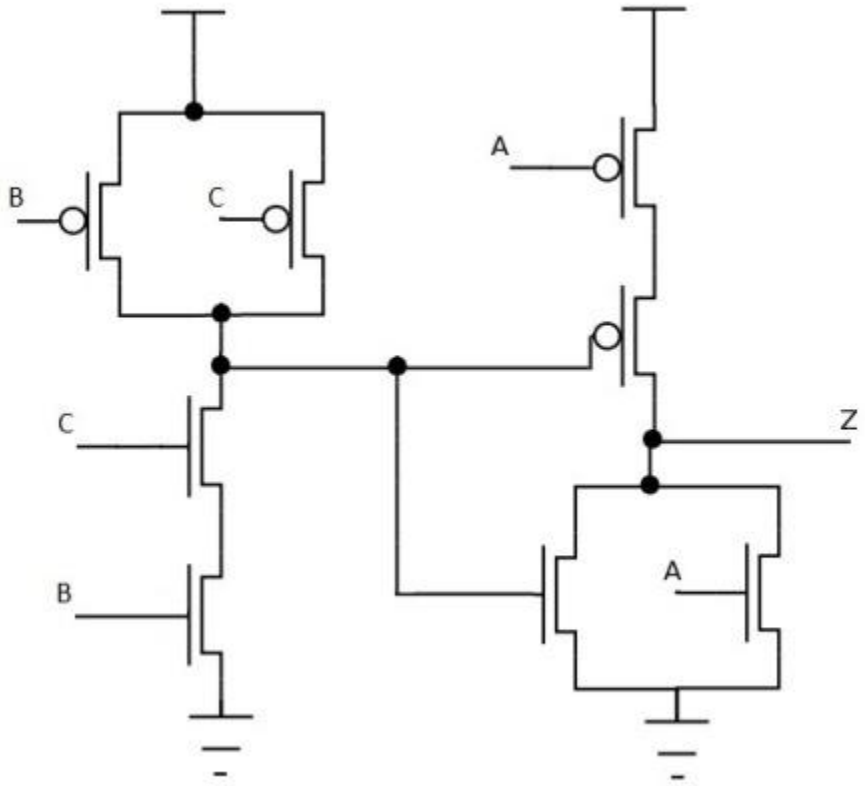
Complete the truth table for the following combinational circuit that uses three 2:1 multiplexers, and has A, B, C as the inputs and Z as the output.



A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Problem 9 **(4 Points)**

Complete the truth table for the following transistor-level circuit, where A, B, C are inputs and Z is the output.



A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Scratch page. You do not need to turn this page in.