CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

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Midterm Examination 3

In Class (50 minutes)

Friday, April 12, 2013

Weight: 17.5%

NO: BOOK(S), NOTE(S), OR CALCULATORS OF ANY SORT.

The exam has 10 pages. **Circle your final answers**. Plan your time carefully since some problems are longer than others. You **must turn in the pages 1-8**. The LC-3 instruction set is provided to you on the last page.

LAST NAME: ____

FIRST NAME: ____

ID# ____

Problem	**Maximum Points**	**Points Earned**
1	4	
2	4	
3	4	
4	3	
5	6	
6	4	
7	5	
Total	30	

Problem 1 **(4 Points)**

For the following questions, select the **best** answer. Choose only **one answer per question**.

i. Which of the following LC-3 instructions can only have register operands and cannot have either immediate or memory operands?

   [✓ a. NOT]
   b. AND
   c. ADD
   d. LD

ii. Which of the following is ***not*** true about branch instructions?

   a. They can change the PC value.
   [✓ b. They change the condition code.]
   c. In LC-3, they can be used for both conditional and unconditional jump.
   d. They can be used to create a loop.

iii. Excluding the memory access to fetch the instruction, which of the following is ***not*** true about the different load instructions in LC3?

   a. LDI instruction makes two memory accesses.
   [✓ b. LEA instruction makes one memory access.]
   c. LD instruction makes one memory access.
   d. LDR instruction makes one memory access.

iv. Apart from incrementing the PC in the fetch stage of an instruction cycle, the processing of which of the following instructions does not perform an addition?

   [✓ a. AND]
   b. STR
   c. ADD
   d. LDR
   e. All of the above.

Problem 2 **(4 Points)**

Give the contents of the following registers after instruction 1 (at address 0x3014) has executed but before the fetch phase of instruction 2 (at address 0x3015) has started.

	Address	**Instruction**
1.	0x3014	0001 0100 0100 0001
2.	0x3015	0001 0110 1000 0010

Program Counter (PC)	0x3015
Instruction Register(IR)	0x1441
Memory Address Register (MAR)	0x3014
Memory Data Register (MDR)	0x1441

Problem 3 **(4 Points)**

We are about to execute the following code snippet. Assume that before execution R6 = 0x2000 and that the value at memory address 0x30A0 = 0x2000. Complete each of the below LC-3 machine instructions so that each instruction stores the value in R2 at the destination address specified in the rightmost column.

Instruction Address	**Instruction**	**Destination Address**
0x3000	0111 010 110 000100	0x2004
0x3001	0011 010 111111101	0x2FFF
0x3002	1011 010 010011101	0x2000

Problem 4 **(3 Points)**

Consider the following LC-3 instructions. The “Intended Operation” specifies what was expected from the Instruction. Identify errors, if any, in the given instructions, and give a brief description of the error in the space provided. Write “No error” in case there is no error in the given instruction.

	Instruction	**Intended Operation**
(a)	0001 011 010 000 010	R3 ← R2 + R1
(b)	1100 010 010 100010	R2 ← R2 AND (0x2)
(c)	1001 001 001 110000	R1 ← NOT(R1)

(a) Yes, there is an error. The result R2 + R2 is stored into R3 rather than R2 + R1

(b) Yes there is an error. The opcode is not the one for AND.

(c) Yes there is an error. Bits 0 to 4 should be all ones for a NOT operation.

Problem 5 **(6 Points)**

We are about to execute the following code snippet:

Address	Instruction	Comment
0x3000	0111 000 001 000101	STR R0, R1, offset = 5 : M[0x2F02] ←R0
0x3001	0010 000 100000000	LD R0, offset = 0xFF00 : R0 ←M[0x2F02]
0x3002	0000 101 000000001	BRnp offset = 1 : R0 is 0, don't branch
0x3003	0001 010 010 000 010	ADD R2, R2, R2 : R2 = 2*R2
0x3004	0011 010 000000010	ST R2, offset = 0x0002 : M[0x3006] ← R2
0x3005	1111 0000 0010 0101	HALT

Assume the following shows the contents of certain parts of memory **before** execution:

Address	Value
0x2F01	0x3000
0x2F02	0x3001
0x2F03	0x3002
0x3006	0x3003
0x3007	0x3004
0x3100	0x3005

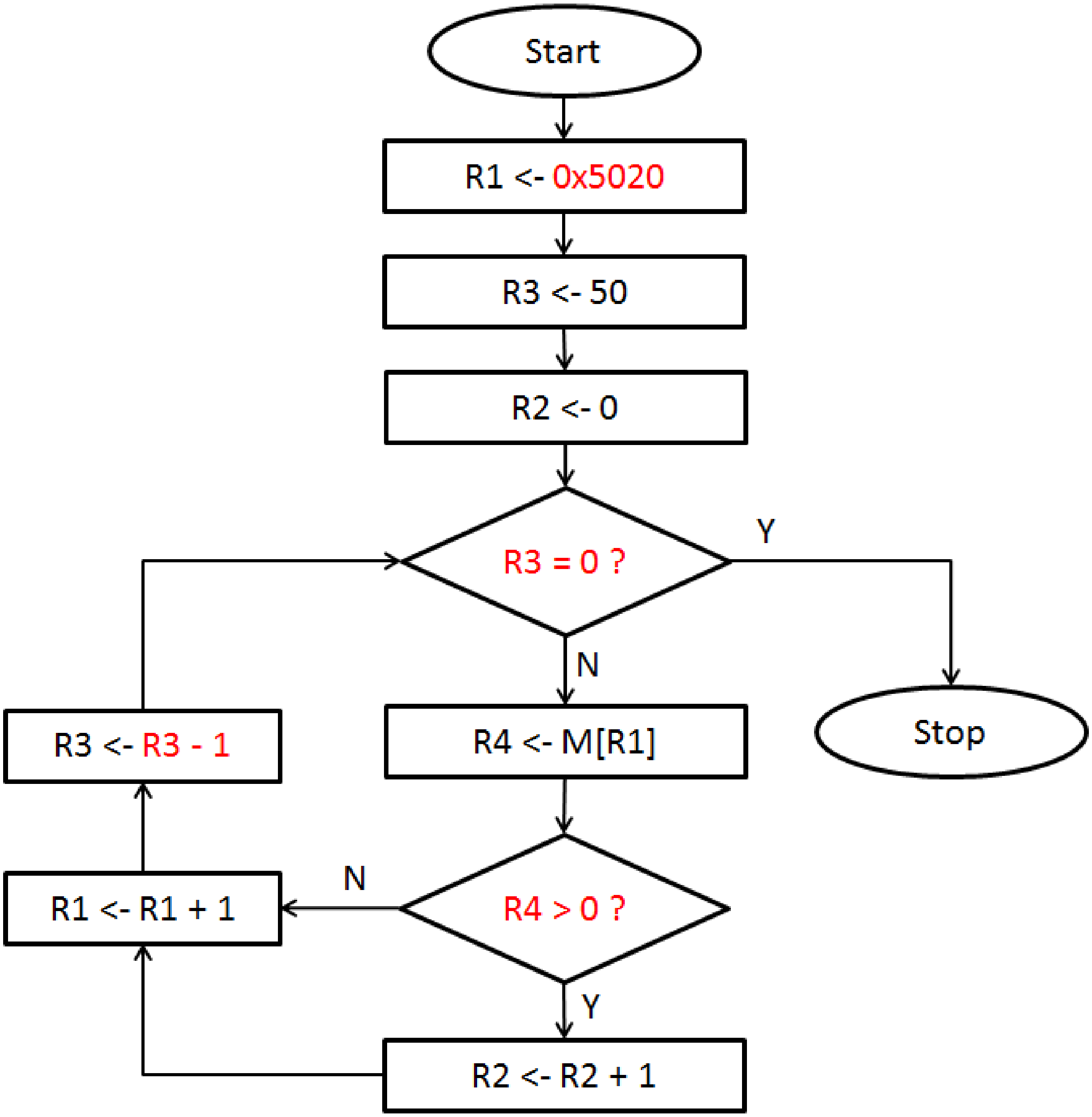
Given the initial values of the below registers, fill in the values after the program has completed execution (before the fetch phase of the HALT). Give your answers in **hex.**

Register	Initial Value	Final Value
CC	N	P
R0	0x0000	0x0000
R1	0x2EFD	0x2EFD
R2	0x0FFF	0x1FFE

Problem 6 **(4 Points)**

The following flowchart represents an algorithm which counts the number of positive numbers stored in 50 consecutive memory locations starting from 0x5020. On completion, it sets the value of register R2 to the count of positive numbers found. Fill in the missing parts of the flowchart indicated by "_______".

Register Usage:
R1: address of stored number, R2: count, R3: number of numbers remaining, and R4: a number.



Problem 7 **(5 Points)**

Answer the following short answer questions using **1-2** sentences.

a. What advantage does the LC-3 LDR instruction provide over the LD instruction? **(1 Point)**

The LDR instruction can address more locations in memory since it uses a register offset which can access 2^{16} locations, whereas LD uses PCoffset which can access 2^9 locations.

b. What is the difference between Breakpoints and Single-Stepping? **(2 Points)**

Breakpoints are used to indicate an instruction to pause at when execution reaches it. Single-stepping is the act of executing one instruction at a time.

c. Name one **non**-memory addressing mode and one memory addressing mode supported by LC-3. Give an example LC-3 OPCODE corresponding to each mode that you list (e.g. ADD, LD, ST). **(2 Points)**

Memory addressing modes:
PC-Relative: LD, ST
Indirect: LDI, STI
Base offset: LDR, STR

Non-memory addressing modes:
Register: ADD, AND, NOT
Immediate: ADD, AND