

Compiling and Simulating Verilog at CS

CS/ECE 552-1

Spring 2005

To set up Mentor for Verilog: (done once)

1. Add the following line to your `~/ .cshrc.local` file:
`setenv MGLS_LICENSE_FILE`
`/s/mentor/etc/cust/mgls/mgc.licenses`
2. Type `source .cshrc` in your home directory
3. `cd $MGC_WD`
This is your main Mentor graphics directory
4. `mkdir vlogcode`
This creates the directory in which you will place your Verilog symbols, created in Design Architect.
5. `mkdir vlogsym`
This creates the directory in which you will place your Verilog symbols, created in Design Architect.
6. `qhlib vloglib`
This creates the directory that will contain the library of all Verilog devices that you create. When you compile a device's Verilog description, the result will be placed here.
7. `qhmap vlog552 $MGC_WD/vloglib`
This tells Mentor to look in the directory that you created in step 4 to find the model information for your devices. You will refer to this model library as "vlog552."

To Create and Compile a Verilog File:

1. `cd $MGC_WD/vlogcode`
2. Create `<yourfile>.v` using your preferred text editor.
3. `vlog -work vlog552 <yourfile>.v`
This compiles the device and places the working model in the library called "vlog552."
4. Fix any errors and repeat step 3.

To Generate a Symbol for the New Device in Design Architect:

1. `da`
This starts Design Architect.
2. `QSPRO->Generate Symbol`
This brings up the symbol creation dialog box. Fill it in with:
Choose source: Module
Library Logical Name: Choose Library->vlog552 (or type vlog552)
Module Name: Choose Module-> `<your new module>`
Directory: `$MGC_WD/vlogsym`
Click "OK"
3. Check and save the symbol.

To Create a Schematic that Uses the New Symbol:

Open a new schematic in Design Architect and click on “Choose Symbol” in the “Schematic: Add/Route” window on the right to add it to the schematic. This creates <schematic dir> as mentioned below.

To Simulate a Design that has Verilog Objects:

1. `cd $MGC_WD`
2. `qhpro <schematic dir> -lib vlog552`

This starts QuickSim II. Be sure to start it this way and not directly. If you start it directly, you will get “model not found” warnings for your devices, since their models are found in “vlog552,” and attached by QhPro.

3. `Solver->QuickSim II`

This menu selection is on the far right.

You can now simulate the design in the normal way. Ignore the additional window that came up.

To Invoke a Force File on this Design:

1. `File->Open Sheet`

This opens a window with the design that you are simulating. You do not have to do this, but it makes the trace window more meaningful if you can see the design.

2. `Setup->Force->From file...`

This allows you to select the force file that you want to apply to this circuit.