

CS/ECE 752 ADVANCED COMPUTER ARCHITECTURE I
HOMEWORK # 3

(Due by 11:59 AM on Monday, March 15, via upload of PDF to Canvas)

Contact Haocheng Xiao (hxiao55@wisc.edu) for questions

1. (20 points) Gem5

For this problem you will be implementing a 4-bit branch predictor. A 4-bit predictor has sixteen states and it is a natural extension of the 2-bit predictor.

Edit *2bit_local.cc* and *BranchPredictor.py* to support the 4-bit prediction scheme with BHT consisting of 2048 entries (number of sets in the local predictor table). For each entry in the prediction buffer, the state of the branch predictor entries should be initialized to 0000 (strongly not taken).

- (a) Using out-of-order CPU model (DerivO3), run the 4-bit predictor with gem5's default configuration (*se.py*). Use the three benchmarks (from HW2).

Fast forward 100M instructions and run for the next 50M instructions for all the benchmarks.

Similarly, run the built-in 2-bit and ltage prediction schemes. Compare and comment on your results of the three policies in terms of IPC and miss rate at the L1 and the L2 cache.

- (b) Include a print-out of the changes to *2bit_local.cc* and *BranchPredictor.py* with your changes highlighted.

2. (30 points)

Consider the following piece of code.

1. ldf X(r1),f1
2. addf f1,f3, f0 ; f0 = f1 + f3
3. ldf X(r2),f1
4. mul f1, f0, f2
5. addi r1,4,r1
6. stf f2,X(r1)
7. slt r1,r3,r4

Assume that the above code is being run on MIPS R10K like out-of-order processors.

- (a) Construct and fill out the following tables after 11 cycles and in the last cycle of the program's execution.

1) ROB

- 2) Reservation Stations
- 3) Map Table
- 4) Free List

(b) For how many cycles does this program run?

Assumptions:

- 1) The processor can dispatch, issue, complete and retire one instruction at a time.
- 2) Floating point multiplication operations take 3 cycles to execute, while floating point add takes 2 cycles (this is only the number of execute cycles and does not include the “complete” cycle).
- 3) All load operations take 3 cycles and store operations take 2 cycles to execute (this is only the number of execute cycles and does not include the “complete” cycle).
- 4) Integer operations take 1 cycle to execute (this is only the number of execute cycles and does not include the “complete” cycle).
- 5) Functional units are fully pipelined.
- 6) There are only 16 physical registers and they can be used to store floating point and integer values.
- 7) There are only 8 ROB slots available and 5 reservation stations.

The tables' status at the end of cycle 2 is as below (note the column for Retire (R) also):

ROB:

ht	#	Inst	T	Told	S	X	C	R
h	1	ldf X(r1),f1	PR#9	PR#2	c2			
t	2	addf f1,f3,f0	PR#10	PR#1				
	3							

Reservation Stations:

#	FU	Busy	op	T	T1	T2
1	ALU	N				
2	L/S1	Y	ldf	PR#9	-	PR#5+
3	L/S2	N				
4	FP1	Y	addf	PR#10	PR#9	PR#4+
5	FP2	N				

Map Table:

f0	PR#10
f1	PR#9
f2	PR#3+
f3	PR#4+
r1	PR#5+
r2	PR#6+

r3 PR#7+
r4 PR#8+

Free List:

PR#11, PR#12, PR#13, PR#14, PR#15, PR#16