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Swapnil D. Haria

Research Interests

Persistent Memory, Virtual Memory, interplay of operating systems and computer architecture

Education

University of Wisconsin-Madison
M.S., Ph.D. Candidate (Computer Sciences), Cumulative GPA – 4.0 *Fall '14 – present*
Courses - Advanced Computer Architecture I, II, Advanced Operating Systems, Ancient Philosophy, etc.
Awarded **CS Departmental Research Fellowship**

Birla Institute of Technology & Science (BITS), Pilani **India**
B.E. (Electrical and Electronics), Cumulative GPA – 10.0/10.0 *Fall '09 – Spring '13*
Awarded **University Gold Medal** and Best Graduating Student Award

Industrial Experience

ORACLE **Santa Clara, CA**
Software Developer [Languages: C] *May '15–Aug '15*
Engaged in kernel development as part of the NUMA/Scheduling team in the Solaris Core Kernel Group
- Investigated the use of hardware performance counters to improve OS scheduling in NUMA/CMT environments
- Developed a self-managing and extensible kernel framework from scratch

NVIDIA **Bangalore, India**
ASIC Engineer [Languages: System Verilog, Verilog, Perl, ARM Assembly] *Jan '13–Jul '14*
Involved in functional verification of Denver CPU (part of 64-bit Tegra K1 SOC)
- Used System Verilog (VMM) for creating and managing testbench infrastructure as unit owner
- Created unit tests in ARMv8 assembly

Research Experience

University of Wisconsin-Madison **Madison**
Research Fellow, Research Assistant [Languages: C, C++, Python, Java] *Fall '14 - present*
Advisors: Prof. Mark Hill and Prof. Michael Swift
- Currently investigating hardware and software techniques for guaranteeing consistency in PM applications
- Helped create first benchmark suite of realistic Persistent Memory (PM) applications
- Developed techniques for simplifying virtual memory support in accelerators

USC Viterbi School of Engineering **Los Angeles**
Research Fellow [Languages: C, Verilog] *Summer '12*
Explored problems in field of networking applications on reconfigurable hardware under Prof. Viktor Prasanna
- Developed virtual router architecture optimized for scalability and power-efficiency
- Created a unified design methodology for optimizing both IPv4/v6 lookup engines

Indira Gandhi Centre for Atomic Research, Kalpakkam **India**
Research Intern [Languages: VHDL] *Summer '11*
Contributed to real-time monitoring system on FPGA by implementing FFT-based analysis in VHDL

Publications

S. Nalli, S. Haria, M. D. Hill, M. M. Swift, H. Volos, and K. Keeton, An Analysis of Persistent Memory Use with WHISPER, *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '17), China*.

Y.-H.E. Yang, Yun Qu, S. Haria, and V.K. Prasanna, Architecture and performance models for scalable IP lookup engines on FPGA, *International Conference on High Performance Switching & Routing, (HPSR '13)*.

S. Haria and V. Prasanna, Optimal mapping of multiple packet lookup schemes onto FPGA, *International Conference on Reconfigurable Computing and FPGAs (ReConFig '13)*.

S. Haria, T. Ganegedara, and V. Prasanna, Power-efficient and scalable virtual router architecture on FPGA, *International Conference on Reconfigurable Computing and FPGAs (ReConFig '12), Mexico*.

Academic Projects

Supporting Virtual Memory in Heterogeneous Systems [C, C++, Python]: Spring '17 – present
- Studying virtual memory overheads for near-memory and in-memory systems

How Applications use Persistent Memory [C, C++, Python]: Fall '16 – Fall '17
- Developed Hands-Off Persistence System to improve programmability and performance of PM workloads
- Collectively assembled a benchmark suite of real-world PM applications to analyze PM usage

Optimizing Client-side Resource Utilization in Public Clouds [C, Java]: Spring '15
- Used application migration and a distributed management framework to improve cloud utilization
- Developed an extensible lightweight simulator to rapidly validate cloud management policies

Exploring CPU-GPU Coherence in Heterogeneous Systems [C++, Python, OpenCL]: Spring '15
- Investigated the relevance of CPU-GPU coherence for current heterogeneous workloads
- Modified conventional solutions to minimize hardware overheads and boost performance

Evaluating Reuse Caches for mobile processors [C++, Python]: Fall '14
- Extended research techniques for improving the area utilization of caches
- Estimated performance, area and power improvements by simulating appropriate workloads

Technical Skills

Languages – C, C++, Java, Python, Perl, Bash, ARM assembly, System Verilog, Verilog

Tools and Simulators – gem5, gem5-GPU, Intel's Pin tool, McPAT, Cacti

Scholastic Honors

Departmental Research Fellowship, University of Wisconsin-Madison

Gold Medallist, Birla Institute of Technology & Science, Pilani

Best Graduating Student Award, Electrical and Electronics Engineering Department, BITS, Pilani

2012 Viterbi-India Program Award (only 10 students selected nation-wide)

Institute Merit Scholarship, BITS, Pilani in all semesters of undergraduate study

Activities

Vice-Chair, ACM Student Chapter, UW-Madison, organized social and technical events for CS students

President, BITS Model United Nations society, organized a popular annual college-level Model UN

Head, Department of Publications and Correspondence, BITS, Pilani, co-ordinated the participation of over 1000 students for the sports and cultural festivals of BITS, Pilani

Member, Corroboration and Review Committee, BITS, Pilani, managed all financial activities of the Students' Union and advisor to all major organizing committees of the Union

Member, Hoofers Sailing Club

Member, BITS Table Tennis team

Interests

- Solving crosswords and other puzzles, playing table tennis, reading and sailing