1620, Monroe St,
Madison, WI 53711
(630) 987 9517
swapnilster@gmail.com
www.pages.cs.wisc.edu/~swapnilh

Swapnil D. Haria

Objective

Interested in working on High-Performance Hardware or Software Systems.

Education

University of Wisconsin-Madison
M.S., Ph.D. (Computer Sciences), Cumulative GPA – 4.0 *Fall '14 – Summer '19*
Thesis: Architecture and Software Support for Persistent and Vast Memory
Courses: Advanced Computer Architecture I, II, Advanced Operating Systems, Business Strategy, etc.
Awarded **2018 Landweber Graduate Fellowship in Distributed Systems**, 2014 Departmental Research Fellowship

Birla Institute of Technology & Science (BITS), Pilani **India**
B.E. (Electrical and Electronics), Cumulative GPA – 10.0/10.0 *Fall '09 – Spring '13*
Awarded **University Gold Medal** and Best Graduating Student Award

Industrial Experience

GOOGLE **Madison, WI**
Software Engineer [Languages: C++] *Sept '19–present*
Work on F1, a high-performance, distributed database

GOOGLE **Madison, WI**
Software Engineering Intern [Languages: C++] *May '18–Aug '18*
Worked on high-performance distributed DRAM key-value store
- Developed concurrent and asynchronous network layer for client-server communication
- Analyzed microarchitectural bottlenecks in production code

ORACLE **Santa Clara, CA**
Software Developer Intern [Languages: C] *May '15–Aug '15*
Engaged in kernel development as part of the NUMA/Scheduling team in the Solaris Core Kernel Group
- Investigated the use of hardware performance counters to improve OS scheduling in NUMA/CMT environments
- Developed a self-managing and extensible kernel framework from scratch

NVIDIA **Bangalore, India**
ASIC Engineer [Languages: System Verilog, Verilog, Perl, ARM Assembly] *Jan '13–Jul '14*
Involved in functional verification of Denver CPU (part of 64-bit Tegra K1 SOC)
- Used System Verilog (VMM) for creating and managing testbench infrastructure as unit owner
- Created unit tests in ARMv8 assembly

Research Experience

University of Wisconsin-Madison **Madison**
Graduate Research Assistant, Fellow [Languages: C, C++, Python] *Fall '14 - Summer '19*
Advisors: Prof. Mark Hill and Prof. Michael Swift
Research focuses on redesigning memory systems for accelerators and non-volatile memory
- Developed techniques for simplifying virtual memory support in accelerators
- Helped create first benchmark suite of realistic Persistent Memory (PM) applications

USC Viterbi School of Engineering **Los Angeles**
Research Fellow [Languages: C, Verilog] *Summer '12*
Explored problems in field of networking applications on reconfigurable hardware under Prof. Viktor Prasanna
- Developed virtual router architecture optimized for scalability and power-efficiency
- Created a unified design methodology for optimizing both IPv4/v6 lookup engines

Indira Gandhi Centre for Atomic Research, Kalpakkam **India**
Research Intern [Languages: VHDL] *Summer '11*
Implemented FFT-based analysis in VHDL as part of real-time monitoring system on FPGA

Publications

S. Haria, M. D. Hill, and M. M. Swift, MOD: Minimally Ordered and Durable Datastructures for Persistent Memory, *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '20)*.

S. Haria, M. D. Hill, and M. M. Swift, Devirtualizing Memory for Heterogeneous Systems, *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '18)*.

S. Nalli, S. Haria, M. D. Hill, M. M. Swift, H. Volos, and K. Keeton, An Analysis of Persistent Memory Use with WHISPER, *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '17), China*. **IEEE Micro Top Picks 2018 Honorable Mention**.

Y.-H.E. Yang, Yun Qu, S. Haria, and V.K. Prasanna, Architecture and performance models for scalable IP lookup engines on FPGA, *International Conference on High Performance Switching & Routing, (HPSR '13)*.

S. Haria and V. Prasanna, Optimal mapping of multiple packet lookup schemes onto FPGA, *International Conference on Reconfigurable Computing and FPGAs (ReConFig '13)*.

S. Haria, T. Ganegedara, and V. Prasanna, Power-efficient and scalable virtual router architecture on FPGA, *International Conference on Reconfigurable Computing and FPGAs (ReConFig '12), Mexico*.

Scholastic Honors

2018 Landweber NCR Graduate Fellowship in Distributed Systems, University of Wisconsin-Madison

2014 Departmental Research Fellowship, University of Wisconsin-Madison

Gold Medallist, Birla Institute of Technology & Science, Pilani

Best Graduating Student Award, Electrical and Electronics Engineering Department, BITS, Pilani

2012 Viterbi-India Program Award (only 10 students selected nation-wide)

Institute Merit Scholarship, BITS, Pilani in all semesters of undergraduate study

Activities

Vice-Chair, ACM Student Chapter, UW-Madison, organized social and technical events for CS students

President, BITS Model United Nations society, organized a popular annual college-level Model UN

Head, Department of Publications and Correspondence, BITS, Pilani, co-ordinated the participation of over 1000 students for the sports and cultural festivals of BITS, Pilani

Member, Corroboration and Review Committee, BITS, Pilani, managed all financial activities of the Students' Union and advisor to all major organizing committees of the Union

Member, Hoofers Sailing Club

Member, BITS Table Tennis team

Technical Skills

Languages – C, C++, Java, Python, Perl, Bash, ARM assembly, System Verilog, Verilog

Tools and Simulators – gem5, gem5-GPU, Intel's Pin tool, McPAT, Cacti

Academic Projects

How Applications use Persistent Memory [C, C++, Python]: Fall '16 – Summer '19
- Developed Hands-Off Persistence System to improve programmability and performance of PM workloads
- Collectively assembled a benchmark suite of real-world PM applications to analyze PM usage

Supporting Virtual Memory in Heterogeneous Systems [C, C++, Python]: Spring '17 – Spring '18
- Studying virtual memory overheads for near-memory and in-memory systems

Optimizing Client-side Resource Utilization in Public Clouds [C, Java]: Spring '15
- Used application migration and a distributed management framework to improve cloud utilization
- Developed an extensible lightweight simulator to rapidly validate cloud management policies

Interests

Solving crosswords and other puzzles, playing table tennis, reading and sailing