Swapnil D. Haria

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Objective

Hoping to work (full-time/intern) on engaging problems in computer architecture or systems

Education

University of Wisconsin-Madison

M.S. (Computer Sciences), Cumulative GPA – 4.0   *Fall '14 – present*

Graduate coursework - Advanced Computer Architecture I, II, Advanced Operating Systems

Awarded **CS Departmental Research Fellowship**

Birla Institute of Technology & Science (BITS), Pilani   **India**

B.E. (Electrical and Electronics), Cumulative GPA – 10.0/10.0   *Fall '09 – Spring '13*

Awarded **University Gold Medal** and Best Graduating Student Award

Industrial Experience

ORACLE   **Santa Clara, CA**

Software Developer   *May '15–Aug '15*

Engaged in kernel development as part of the NUMA/Scheduling team in the Solaris Core Kernel Group

○ Investigated the use of hardware performance counters to improve OS scheduling in NUMA/CMT environments
○ Developed a self-managing and extensible kernel framework from scratch

NVIDIA   **Bangalore, India**

ASIC Engineer   *Jan '13–Jul '14*

Involved in functional verification of Denver CPU (part of 64-bit Tegra K1 SOC)

○ Witnessed computer architecture principles in action, specifically in core and Design for Debug (DFD) blocks
○ Used System Verilog (VMM) for creating and managing testbench infrastructure as unit owner

Research Experience

University of Wisconsin-Madison   **Madison**

Departmental Research Fellow, Research Assistant   *Fall '14 - present*

Developing techniques to minimize virtual memory overheads for managed languages

USC Viterbi School of Engineering   **Los Angeles**

Research Fellow   *Summer '12*

Explored problems in field of networking applications on reconfigurable hardware under Professor Viktor Prasanna

Academic Projects

Optimizing Client-side Resource Utilization in Public Clouds: Spring '15

○ Used application migration and a distributed management framework to improve cloud utilization
○ Developed an extensible lightweight simulator to rapidly validate cloud management policies

Exploring CPU-GPU Coherence in heterogeneous systems: Spring '15

○ Investigated the relevance of CPU-GPU coherence for current heterogeneous workloads
○ Modified conventional solutions to minimize hardware overheads and boost performance

Activities

President, BITS Model United Nations society, organized a popular annual college-level Model UN

Member, Corroboration and Review Committee, BITS, Pilani, managed all financial activities of the Students' Union and advisor to all major organizing committees of the Union

Technical Skills

Languages – System Verilog, Verilog, C, C++, Java, Scheme, Python, Perl, Bash, ARM Assembly

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