VINAY GANGADHAR

Graduate Research Assistant, UW-Madison

Madison, WI
+1 (608)-358-5157
vinay@cs.wisc.edu
www.linkedin.com/in/vinaygangadhar
pages.cs.wisc.edu/~vinay/

Research Summary

- Hardware/Software co-design of novel energy-efficient accelerators
- Coarse and fine-grained specialization mechanisms in accelerators
- Open-source hardware design of programmable accelerators and interfaces
- GPGPU computing and micro-architecture

Education

PhD in Electrical and Computer Engineering
Jan 2015 - Dec 2018

University of Wisconsin-Madison

Computer Architecture Specialization | Under the supervision of Dr. Karu Sankaralingam

Master of Science (M.Sc) in Electrical and Computer Engineering
Aug 2012 - Aug 2016

University of Wisconsin-Madison

Computer Architecture Specialization, CGPA: 3.79/4

Relevant Coursework: Digital System Design and Synthesis using Verilog, Introduction to Computer Architecture, Advanced Computer Architecture I, Advanced Computer Architecture II, Introduction to Operating Systems, Advanced Compilers, Advanced Operating Systems, Embedded Computing Systems and High Performance Computing

Bachelor of Engineering (B.E) in Electronics and Communication
Aug 2007 - June 2011

Visvesvaraya Technological University, India

CGPA: 9.18/10

Work History

Research Intern
May 2016 - Aug 2016

Microsoft Research, Redmond, WA

Energy-efficient programmable acceleration on the reconfigurable logic of chip multi-processors using novel micro-architectural execution mechanisms.

Graphics Architecture Software Intern
June 2013 - Jan 2014

Intel Corporation, Folsom, CA

Developed a performance analysis tool (pipetrace), to analyze the micro-architectural transactions/events in Intel's next generation GPU graphics pipeline.

Contract Developer
Feb 2012 - May 2012

Oracle Corporation, Hyderabad, India

ETL developer and part of an OBIEE (Business Analytics) team developing data analytics toolchain.

Associate Consultant

June 2011 - Feb 2012

Frontline Consulting Services (FCS) Inc, Hyderabad, India

Consultant Development of ETL mappings for transactional databases.

Academic Experience

Graduate Research Assistant

Jan 2013 - Present

University of Wisconsin Madison, Vertical Research Group

- Design and implementation of energy-efficient programmable accelerators and specialization engines. Hardware/software co-design approached for efficient mapping of application kernels to the accelerators.
- Contributions to a new von neumann/dataflow hybrid architecture to exploit ILP in irregular applications.
- One of the lead developers and active contributor to an Open Source RTL implementation of a GPGPU based on AMD SI ISA. Project link - http://www.miaowgpu.org

Teaching Assistant

Jan 2013 - June 2013

University of Wisconsin Madison, Department of Computer Sciences

Worked with Professor Karu Sankaralingam to develop curriculum for Introduction to Computer Architecture course (ECE/CS 552). Responsible for developing and grading the projects of students.

Teaching Assistant

Sep 2012 - Dec 2012

University of Wisconsin Madison, Department of Mathematics

Worked with Prof. Gregory Shinault for Linear Algebra and Differential Equations course. Responsible for handling discussion classes and grading the exam papers.

Academic Publications

- G. Gupta, T. Nowatzki, **V. Gangadhar** and K. Sankaralingam. Open-source Hardware: Opportunities and Challenges. *To appear in IEEE Computer 2016.*
- T. Nowatzki, **V. Gangadhar** and K. Sankaralingam. Pushing the Limits of Efficiency While Retaining the General-purpose Programmability. *Appeared in 22nd International Symposium on High-Performance Computer Architecture (HPCA-22), Barcelona, Spain, March 12-16 2016.*
- T. Nowatzki, **V. Gangadhar** and K. Sankaralingam. A Heterogeneous Von Neumann/Explicit Dataflow Processor. *IEEE-Micro TopPicks 2016 (Volume 36; Issue:3), May-June 2016.*
- T. Nowatzki, **V. Gangadhar** and K. Sankaralingam. Exploring the potential of Heterogeneous Von Neumann/Dataflow Execution Models. *Appeared in 42nd International Symposium on Computer Architecture (ISCA), Portland, OR, June 13-17 2015.*
- R. Balasubramanian, V. Gangadhar, Z. Guo, C. Ho, C. Joseph, J. Menon, M. Drumond, R. Paul, S. Prasad, P. Valathol, and K. Sankaralingam.
  - MIAOW - An Open Source RTL Implementation of a GPGPU. *In COOL Chips XVIII: Proceedings of the International Symposium on Low-Power and High-Speed Chips, Yokohama, Japan, April 14-17 2015.*
  - Enabling GPGPU Low-level Hardware Explorations with MIAOW - An Open Source RTL Implementation of a GPGPU. In ACM Transactions on Architecture and Code Optimization (TACO), Volume 12 Issue 2, July 2015, Article No. 21.
  - MIAOW - An Open Source GPGPU. *In Hot Chips 27: A Symposium on High Performance Chips, Cupertino, CA, August 23-25 2015.*

Skills

Programming

C, C++, Verilog, VHDL, Python, Perl, Scala and Shell Scripting

Architectural Simulators

Gem5, Multi2Sim, CACTI, SimpleScalar, McPAT

Toolchains

RISCV toolchain, LLVM Compiler, CUDA, OpenCL, Chisel, Arduino IDE, Xilinx EDK/SDK and Synopsys tools (DC, DV, VCS)

Academic Projects

- Embedded Computing Systems: Design of a programmable engine for neural networks.
- Advanced Operating Systems: Efficient Energy Management policies in OS (E-MOS).
- Compiler Optimizations: Dataflow analysis, Loop invariant code motion, Reaching definition analysis and Register allocation using Graph coloring.
- Operating Systems Projects: Command line interpreter (Shell console), Memory management library, Scalable web-server and Network file server.
- Advanced Comp. Arch I: Evaluation of Modern Microprocessor Architectures for Simultaneous Multithreading (SMT).
- Advanced Comp. Arch II: Reevaluating the Two Hop Protocols for On-Chip Multi-core Cache Coherence.
- Introduction to Computer Architecture: Design of a 16bit Single Cycle 5 Stage Pipelined processor using Verilog / Quartus Digital System.
- Digital Design and Synthesis: High Speed Calibratable Angle Resolver (CAR) using Verilog.