

# Bijan Tabatabai

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## Education:

- **University of Wisconsin-Madison**, Madison, WI (In Progress, Sept 2020 - Present)
  - PhD in Computer Sciences, Advised by Prof. Michael Swift
- **University of Wisconsin-Madison**, Madison, WI (September 2015 – May 2020)
  - BS in Computer Sciences and Electrical Engineering
  - Cumulative GPA: 3.9

## Research:

- Graduate Research Assistant advised by Prof. Michael Swift (September 2020 – Present)
  - Researched how to make kernel memory management operations more consistent
    - Replaced existing memory management heuristics with more principled policies
    - Profiled applications to generate a cost-benefit model for MM policies
  - Currently researching how file system block allocators perform when used to allocate anonymous memory

## Previous Work Experience:

- Software Engineering Intern, Ocient Inc. (June 2022 – August 2022)
  - Optimized use of bloom filters in a database application.
- Embedded Software Co-Op, Extreme Engineering Solutions. (May 2018 – August 2020)
  - Maintained support for U-Boot boot loader on single board computers
  - Performed rigorous release testing to ensure working software for production
- Firmware Intern, Northstar Medical Radioisotopes. (May 2017 – August 2017)
  - Wrote firmware for medical devices in the C programming language.
  - Ported legacy code into C.
  - Used oscilloscope to debug the firmware.
- Application Developer Intern, BD Gencell. (June 2015 – June 2016)
  - Wrote drivers to communicate with various sensors and controllers.

## Publications:

- Mark Mansi, **Bijan Tabatabai**, Michael M. Swift. CBMM: Financial Advice for Kernel Memory Managers. ATC 2022.

## Skills:

- C, C++, Java, Rust, C#, Python, Git
- Experience working in Linux and Windows environments
- Experience modifying the Linux Kernel
- Experience writing embedded software

## Extracurricular Activities:

- FeRTOS
  - Hobby software library inspired by FreeRTOS written in Rust
  - Allows for time-multiplexed tasks in embedded systems
  - Includes semaphores and inter-task message passing
  - Supports Arm Cortex-M and RISC-V processors