JICHUAN CHANG

1210 W. Dayton Street Computer Sciences Department University of Wisconsin-Madison Madison, WI 53706 Phone: (608) 262-6618
Fax: (608) 262-9777
Email: chang@cs.wisc.edu
http://www.cs.wisc.edu/~chang

RESEARCH INTERESTS

Computer architecture: focusing on cache/memory hierarchy design for multicore systems; cache coherence, synchronization and value communication; and hardware support to improve programmability and reliability.

EDUCATION

Ph.D. (Expected February 2007) Computer Sciences Department, University of Wisconsin-Madison. Advisor: Professor Guri Sohi. Dissertation: Cooperative Caching for Chip Multiprocessors.
 M.Sc. in Computer Sciences University of Wisconsin-Madison. May 2003. GPA: 4.0/4.0.
 B.Sc. in Computer Sciences Peking University. July 2000. GPA: 3.95/4.0.
 Peking University. July 1997. GPA: 3.86/4.0.

RESEARCH EXPERIENCES

Graduate Research Assistant. Multiscalar group. University of Wisconsin-Madison. June 2002—present.

♦ Cache coherence and synchronization, multicore caching and cache partitioning.

Graduate Research Assistant. Condor project. University of Wisconsin-Madison. June 2001—June 2002.

♦ Middleware and programming framework for master-worker (MW) style parallel computing.

Graduate Research Assistant. ABLE project. Carnegie Mellon University. July 2000—June 2001.

♦ Software architecture based introspection and adaptation.

Graduate Research Assistant. Software Engineering Institute. Peking University. July 1999—July 2000.

♦ Software architecture, software component composition, object-oriented middleware.

Graduate Teaching Assistant. Undergraduate operating systems. Peking University. Fall 1998.

PUBLICATIONS Available at http://www.cs.wisc.edu/~chang/publications.html

- **Jichuan Chang** and Gurindar S. Sohi, "Cooperative Cache Partitioning for Chip Multiprocessors," under submission for publication.
- **Jichuan Chang** and Gurindar S. Sohi, "Cooperative Caching for Chip Multiprocessors," 33rd Annual International Symposium on Computer Architecture (ISCA-33), June 2006.
- Jaehyuk Huh, Doug Burger, **Jichuan Chang** and Gurindar S. Sohi, "Speculative Incoherent Cache Protocols," IEEE Micro 24(6): **Micro's Top Picks**, November-December 2004.
- Jaehyuk Huh, **Jichuan Chang**, Doug Burger and Gurindar S. Sohi, "Coherence Decoupling: Making Use of Incoherence," 11th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XI), October 2004.
- **Jichuan Chang**, Jaehyuk Huh, Rajagopalan Desikan, Doug Burger and Gurindar S. Sohi, "Using Coherent Value Speculation to Improve Multiprocessor Performance," First Value Prediction Workshop, June 2003.
- David Garlan, Bradley Schmerl and **Jichuan Chang**, "Using Gauges for Architecture-based Monitoring and Adaptation," Working Conference on Complex and Dynamic Systems Architecture, December 2001.

PROFESSIONAL SKILLS

- Computer Languages/Platforms: C, C++, Java, Pascal, Visual Basic, Excel, assembly languages, scripting languages; MS Windows/DOS, Unix/Linux, Solaris; Simics and Simics/MAI.
- **Software Engineering Experiences:** Object-oriented analysis and design, GUI development, project management and processor improvement, software architecture evaluation.

REFERENCES Available upon request.