

CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING
COMPUTER SCIENCES DEPARTMENT
UNIVERSITY OF WISCONSIN-MADISON

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Midterm Examination 3
In Class (50 minutes)
Monday, April 21, 2008
Weight: 15%

CLOSED BOOK, NOTE, CALCULATOR, PHONE, & COMPUTER.

The exam is two-sided and has **10** pages, including two blank pages and a copy of the *LC-3 Instruction Set handout* on the final page (please feel free to detach this final page, but insert it into your exam when you turn it in).

You are **required** to present a valid UW-Madison student ID card or other government-issued photo ID to one of the teaching assistants who are proctoring this exam before leaving the room. **If you fail to do so, we cannot grade your exam.**

Plan your time carefully, since some problems are longer than others.

NAME: _____

ID# _____

Problem Number	Maximum Points	Points Awarded
1	12	
2	9	
3	15	
4	24	
5	20	
6	10	
7	10	
Total	100	

Problem 1 (12 points)

The following LC-3 program has been loaded into memory:

Address	Instruction
x5000	1001 0010 0011 1111
x5001	0001 0010 0110 0001
x5002	0001 0010 0100 0010
x5003	0000 0110 0000 0110

a) The contents of the registers are shown below:

R0 is 4 R1 is 3 R2 is 0 R3 is 5

Which condition codes are set and what is the value of the PC after instruction at x5003 is executed?

b) The contents of the registers are shown below:

R0 is 3 R1 is 0 R2 is 5 R3 is 4

Which condition codes are set and what is the value of the PC after instruction at x5003 is executed?

Problem 2 (9 points)

The contents of the memory and the registers are shown below:

Register	Value	Memory address	Value
R0	x3012	x3010	x3012
R1	x002A	x3011	x3010
R2	x300B	x3012	xBEEF

We start executing from address x3000. What 's the value in R1 after each instruction is executed?

- a) If x3000 is 0010 0010 0001 0000 LD R1, PTR
- b) If x3000 is 0110 0010 1000 0111 LDR R1, 7(R2)
- c) If x3000 is 1010 0010 0001 0000 LDI R1, PTR

Problem 3 (15 points)

The program below sums a sequence of numbers. The address to the start of the sequence is stored in R2 and the number of elements in that sequence is stored in R3. Insert the missing LC-3 machine language instructions. Adding comments to each machine language instruction will assist in awarding partial credit.

Address	Instruction
x5000	0101 1111 1110 0000 ; AND R7,R7,#0
x5001	0110 0010 1000 0000 ; LDR R1,R2,#0
x5002	0001 1111 1100 0001 ; ADD R7,R7,R1
x5003	
x5004	0001 0110 1111 1111 ; ADD R3,R3,#- 1

x5005

x5006

1111 0000 0010 0101 ; HALT

Problem 4 (24 points)

There is something wrong with the following code. This code is supposed to count the number of positive numbers in a sequence, save this number in R7 and then exit. The sequence always has 10 elements and the address of the start of the sequence has been stored in register R2.

Address	Instruction
x3005	0101 0000 0010 0000 ; AND R0, R0, #0
x3006	0001 0000 0010 1010 ; ADD R0, R0, #10
x3007	0101 1111 1110 0000 ; AND R7, R7, #0
x3008	0110 0010 1000 0000 ; LDR R1, R2, #0
x3009	0000 0010 0000 0001 ; BRp #1
x300A	0001 1111 1110 0001 ; ADD R7, R7, #1
x300B	0001 0100 1010 0001 ; ADD R2, R2, #1
x300C	0001 0000 0011 1111 ; ADD R0, R0, #-1
x300D	0000 0011 1111 1010 ; BRp #-6
x300E	1111 0000 0010 0101 ; HALT

Explain what happens when we try to execute this code. Comments are provided to save you the effort of decoding the machine language.

If you had a debugger, briefly describe how you would use it to debug this program.

Problem 5 (20 points)

The current state of the memory is given below:

Memory Address	Memory Contents
x3006	xABCD
xABCD	x1220
x2FFF	x4567
x1220	x9876
xABDB	x0001
x30F3	x0020
x200E	x3258
x3258	x0000
x300E	x92FE
x3005	x200E

We load and execute the following program:

Address	Instruction
x3000	1010 0000 0000 0101
x3001	0110 0110 0000 0000 ; LDR R3, R0, x0
x3002	1110 0010 1111 0000
x3003	0010 0101 1111 1110 ; LD R2, x1FE
x3004	1111 0000 0010 0101

What will be the final contents of registers R0-R3 when we reach the HALT instruction? Write your answers in hexadecimal format.

Register	Initial contents	Final contents
R0	x200E	
R1	x200E	
R2	x3001	
R3	x3001	

Problem 6 (10 points)

If the value stored in R0 is 1 at the end of the execution of the following instructions, what can be inferred about R3?

Address	Instruction
x4000	1110 0011 1111 1111
x4001	0101 0000 0010 0000 AND R0, R0, x0
x4002	0001 0100 0100 0001
x4003	0101 0110 1000 0011
x4004	0000 0100 0000 0001
x4005	0001 0000 0010 0001 ADD R0, R0, x1

- a. R3 is negative
- b. R3 is positive
- c. R3 is equal to 0
- d. R3 is zero or positive

Problem 7 (10 points)

What does the following instruction sequence do?

Address	Instruction
x4000	1110 0000 0001 0000
x4001	1100 0000 0000 0000

Can you do the same using a single instruction only? If yes, which one? If no, why?

Scratch Sheet 1 (in case you need additional space for some of your answers)

Scratch Sheet 2 (in case you need additional space for some of your answers)

LC-3 Instruction Set (Entered by Mark D. Hill on 03/14/2007; last update 03/15/2007)

PC': incremented PC. setcc(): set condition codes N, Z, and P. mem[A]:memory contents at address A.
 SEXT(immediate): sign-extend immediate to 16 bits. ZEXT(immediate): zero-extend immediate to 16 bits.
 Page 2 has an ASCII character table.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																ADD DR, SR1, SR2 ; Addition		
0	0	0	1	DR		SR1	0	0	0		SR2							
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← SR1 + SR2 also setcc()		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																ADD DR, SR1, imm5 ; Addition with Immediate		
0	0	0	1	DR		SR1	1		imm5									
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← SR1 + SEXT(imm5) also setcc()		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																AND DR, SR1, SR2 ; Bit-wise AND		
0	1	0	1	DR		SR1	0	0	0		SR2							
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← SR1 AND SR2 also setcc()		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																AND DR, SR1, imm5 ; Bit-wise AND with Immediate		
0	1	0	1	DR		SR1	1		imm5									
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← SR1 AND SEXT(imm5) also setcc()		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																BRx, label (where x = {n,z,p,zp,np,nz,nzp}) ; Branch		
0	0	0	0	n	z	p		PCoffset9					GO ← ((n and N) OR (z AND Z) OR (p AND P))					
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																if (GO is true) then PC ← PC' + SEXT(PCoffset9)		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																JMP BaseR ; Jump		
1	1	0	0	0	0	0		BaseR	0	0	0	0	0	0	0			
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																PC ← BaseR		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																JSR label ; Jump to Subroutine		
0	1	0	0	1		PCoffset11												
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																R7 ← PC', PC ← PC' + SEXT(PCoffset11)		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																JSRR BaseR ; Jump to Subroutine in Register		
0	1	0	0	0	0	0		BaseR	0	0	0	0	0	0	0			
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																temp ← PC', PC ← BaseR, R7 ← temp		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																LD DR, label ; Load PC-Relative		
0	0	1	0	DR		PCoffset9												
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← mem[PC' + SEXT(PCoffset9)] also setcc()		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																LDI DR, label ; Load Indirect		
1	0	1	0	DR		PCoffset9												
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← mem[mem[PC' + SEXT(PCoffset9)]] also setcc()		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																LDR DR, BaseR, offset6 ; Load Base+Offset		
0	1	1	0	DR		BaseR		offset6										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← mem[BaseR + SEXT(offset6)] also setcc()		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																LEA, DR, label ; Load Effective Address		
1	1	1	0	DR		PCoffset9												
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← PC' + SEXT(PCoffset9) also setcc()		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																NOT DR, SR ; Bit-wise Complement		
1	0	0	1	DR		SR	1	1	1	1	1	1	1	1	1			
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← NOT(SR) also setcc()		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																RET ; Return from Subroutine		
1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0			
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																PC ← R7		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																RTI ; Return from Interrupt		
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																See textbook (2 nd Ed. page 537).		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																ST SR, label ; Store PC-Relative		
0	0	1	1	SR		PCoffset9												
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																mem[PC' + SEXT(PCoffset9)] ← SR		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																STI, SR, label ; Store Indirect		
1	0	1	1	SR		PCoffset9												
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																mem[mem[PC' + SEXT(PCoffset9)]] ← SR		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																STR SR, BaseR, offset6 ; Store Base+Offset		
0	1	1	1	SR		BaseR		offset6										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																mem[BaseR + SEXT(offset6)] ← SR		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																TRAP ; System Call		
1	1	1	1	0	0	0	0		trapvect8									
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																R7 ← PC', PC ← mem[ZEXT(trapvect8)]		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																; Unused Opcode		
1	1	0	1															
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																Initiate illegal opcode exception		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			