Oct tools

- The **Oct** tools are a suite of **VLSI CAD** programs for **integrated circuit** design.
  - Written at the University of California, Berkeley.
  - The **Oct** tools support a variety of VLSI design styles.
    - Hardware description language.
    - Schematic capture.
    - Netlist entry.
    - Symbolic layout.
    - Physical layout.

Oct tools

- VLSI design example:
  - Using a **hardware description language**, the functionality for a BCD[1] to 7 segment display converter is written.

```
model bcd_7seg seg<6:0> = data<3:0>;
routine decode;
 select data from
  [0#16]: seg=7E#16;
  [1#16]: seg=30#16;
  [2#16]: seg=6D#16;
  [3#16]: seg=79#16;
  [4#16]: seg=33#16;
  [5#16]: seg=5B#16;
  [6#16]: seg=5F#16;
  [7#16]: seg=70#16;
  [8#16]: seg=7F#16;
  [9#16]: seg=7B#16;
  [otherwise]: seg=00#16;
 endselect;
endroutine;
endmodel;
```

[1] **B**inary **C**oded **D**ecimal

Oct tools

- The **Oct** logic optimizer, **misII**, is used to optimize the logic and map the function into existing cells.
  - For this example, the Mississippi State University cell library will be used.
  - There are other options, including:
    - PLA (**P**rogrammable **L**ogic **A**rray).
    - Gate Matrix.

Oct tools

- The simulator, **musa** is used to verify the logic is correct.
  - The logic is "wired" to a simulated display to verify the outputs are correct.
  - As different input values are provided to the simulator, the designer verifies the outputs are as expected.

Oct tools

- The **Oct** place and route program, **wolfe**, is used to create the final layout for the logic.
- The **Oct** graphics editor, **vem**, is used to examine the resulting chip layout.

CMOS Integrated Circuit Design

- Integrated circuits (**chips**) are fabricated via a photolithographic process, using a series of **layers**.
- **Vem** can be used to demonstrate how the individual layers are combined to complete the layout of the chip.

  1 **WELL**

  * The first layer in the process is the **well**. The orange areas define the N-well.

- For this example, the larger **vem** window shows the entire decoder layout. The smaller window is "zoomed in" to a single inverter in the layout.

CMOS Integrated Circuit Design

- Integrated circuits (**chips**) are fabricated via a photolithographic process, using a series of **layers**.
- **Vem** can be used to demonstrate how the individual layers are combined to complete the layout of the chip.

  1 Well

  2 **ACTIVE AREA**

    * The next layer is **Active Area**. This defines the source and drain regions. The brown areas will become P-type, while the green areas will become N-type.

CMOS Integrated Circuit Design

- Integrated circuits (**chips**) are fabricated via a photolithographic process, using a series of **layers**.
- **Vem** can be used to demonstrate how the individual layers are combined to complete the layout of the chip.
  1 Well
  2 Active Area
  3 **POLYSILICON**
    * The next layer is **Polysilicon**. This defines the gate regions for each transistor. The red areas are polysilicon. Polysilicon over P-type active creates a PMOS transistor, while polysilicon over N-type active creates an NMOS transistor.

CMOS Integrated Circuit Design

- Integrated circuits (**chips**) are fabricated via a photolithographic process, using a series of **layers**.
- **Vem** can be used to demonstrate how the individual layers are combined to complete the layout of the chip.
  1 Well
  2 Active Area
  3 Polysilicon
  4 **CONTACTS**
     * The next layer is **Contacts**. Each layer is separated by a layer of insulating glass. The contact layer defines areas where the insulator will be removed to allow electrical contact to the layer.

CMOS Integrated Circuit Design

- Integrated circuits (**chips**) are fabricated via a photolithographic process, using a series of **layers**.
- **Vem** can be used to demonstrate how the individual layers are combined to complete the layout of the chip.
  1 Well
  2 Active Area
  3 Polysilicon
  4 Contacts
  5 **FIRST METAL**
     * The next layer is **First Metal**. Metal is used to interconnect the transistors to form logic gates, which implement the desired function. Where first metal passes over a contact, it is electrically connected to the layer under the contact.

CMOS Integrated Circuit Design

- Integrated circuits (**chips**) are fabricated via a photolithographic process, using a series of **layers**.
- **Vem** can be used to demonstrate how the individual layers are combined to complete the layout of the chip.

  1 Well

  2 Active Area

  3 Polysilicon

  4 Contacts

  5 First Metal

  6 **VIA**

     * The next layer is **Via**. A second layer of metal will soon be added, after first metal is covered with an insulator. The via layer defines areas where the insulator will be removed to create an electrical connection between the metal layers.

CMOS Integrated Circuit Design

- Integrated circuits (**chips**) are fabricated via a photolithographic process, using a series of **layers**.
- **Vem** can be used to demonstrate how the individual layers are combined to complete the layout of the chip.
  1 Well
  2 Active Area
  3 Polysilicon
  4 Contacts
  5 First Metal
  6 Via
  7 **SECOND METAL**
    * The next layer is **Second Metal**. This completes the interconnections. Where second metal crosses a via, it is electrically connected to first metal, otherwise it is insulated from the layers below.

Oct tools

- The **Oct** tools support a variety of design entry methods.
- Tutorials are provided by UC Berkeley and the Massachusetts Microelectronics Center (M^2C) to assist the new user.
  - **Physical Editing**

Oct tools

- The **Oct** tools support a variety of design entry methods.
- Tutorials are provided by UC Berkeley and the Massachusetts Microelectronics Center (M^2C) to assist the new user.
  - Physical Editing
  - **Symbolic Editing**

Oct tools

- The **Oct** tools support a variety of design entry methods.
- Tutorials are provided by UC Berkeley and the Massachusetts Microelectronics Center (M^2C) to assist the new user.
  - Physical Editing
  - Symbolic Editing
  - **Schematic Capture**

Oct tools

- The **Oct** tools support a variety of design entry methods.
- Tutorials are provided by UC Berkeley and the Massachusetts Microelectronics Center (M^2C) to assist the new user.
  - Physical Editing
  - Symbolic Editing
  - Schematic Capture
  - **Hardware Description Language**