Contents

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Cell Data Pages

The cell data pages contain multiple pages of data for each cell as follows:

- Page 1: Terminal information, logic equation, truth table.
- Page 2: Transistor schematic.
- Page 3: Device sizes.
- Page 4: Cell Timing.
- Page 5: Spice deck.

Terminal Information. The terminal name, terminal number and Y-location in lambda (from 0,0) are provided along with input and output classes. Input terminals that have the same class are logically equivalent. All input and output terminals are metal1 to metal2 vias.

Logic Equations. The relevant logic equations are provided using the appropriate terminal names.

Truth Table. A three state input (1,0,- = don’t care), four state output (1,0,- = don’t care, Z = high impedance) truth table is provided for each cell. Inputs “h2l” and “l2h” indicate an edge triggered device and stand for input high-to-low and input low-to-high transitions respectively.

Circuit Schematic. A generic transistor level circuit schematic is provided with the appropriate terminal names. The schematics are electrically true representations of the cell layouts. Transistor numbers match the numbers on the associated cell plots. For complex cells, the schematics may be difficult to read. In this case and in any situations concerning connectivity, consult the spice decks provided, as they were extracted directly from the layouts. Also, the logic symbol for each cell is provided with the appropriate terminal names.

Device Size Table. A table of transistor device numbers with appropriate widths and lengths in lambda is provided for most cells.

Cell Timing. The worst and nominal case cell timing is provided for both 2µ and 3µ at loaded (1 pF) and no load conditions. The delay and rise/fall time from each input class to each output is provided, for both a 0’ 1 and a 1’ 0 output transition. Note that the delay and rise/fall times may be precipitated from two different inputs with the same class.

Spice Deck. A spice deck extracted directly from the cell layout using an interactive MAGIC utility developed at ITD/AµE is provided showing transistor connectivity and capacitance. In later versions of the data book, the capacitance values will not be included in the spice decks, as they are dependent upon the MAGIC technology file being used.

Special Flip-Flop Timing. The four flip-flop cells in the library have an additional page containing setup and hold times and minimum pulse width data for both 2µ and 3µ.

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Cell Layout

Cells must adhere to strict layout rules in order to allow for the placement of cells with their side edges abutting, to allow for the proper connection of inter-cell wiring to the top and bottom cell edges, and to remain compatible with various automatic place and route programs.

All terminals fall on incremental spacings of 8-lambda. A cell is designed using an 8-lambda grid with the first possible terminal location being 4-lambda in from the left edge of the cell. This first possible terminal location is denoted as grid 1 and numbers increase from left to right. A grid that is not used by a terminal or blocked by internal cell wiring can be used as a metal2 feedthru path. Only one terminal exists for each pin name (input or output) and is located internally to the cell. The Y-Location of each terminal is provided in the cell data and indicates the distance, in lambda, from the bottom edge of the cell to the center of the via.

Power busses are included within each cell. Each bus runs horizontally in metal1 and is 8-lambda wide in dlmV2.0. The bus router should route an 8-lambda wide bus to the cell rows, centered accordingly. The bottom (GND) bus is centered on a Y-Offset of 7-lambda. The top (VDD) bus is centered on a Y-Offset of 65-lambda.

The reference point (origin) for all cells is the lower left hand corner of the cell (3-lambda below GND bus). All cells currently have a height of 66-lambda and a width which is a multiple of 8-lambda. As indicated above, an 8-lambda terminal-to-terminal spacing has been maintained for the library. The cells are structured to allow placement of any cell adjacent to another cell with power busses abutting accordingly.

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Cell Library Description

The ITD/AμE SCMOS Standard Cell Libraries are libraries of SSI and MSI cells designed in the MOSIS Scalable CMOS (SCMOS) Design Rules. The cell libraries can be scaled from 3.0 to 1.2 micron CMOS technologies or most technologies in between. The libraries can be scaled to the foundry's technology and characterized around that technology by ITD/AμE. The ITD/AμE SCMOS Cell Libraries have been designed to be compatible with most commercially available standard cell place and route systems.

The ITD/AμE SCMOS Standard Cell Libraries are actually three libraries sharing a common circuit design. The three libraries are:

- **dlmV1.0**: Original library. Transistors have corners (90^{o} turns). Designed under MOSIS Rev4 design rules.
- **dlmV1.1**: Contains straight transistors and additional well plugs.
- **dlmV2.0**: Reduced cell height (from 100-lambda to 66-lambda). Also contains straight transistors and additional well plugs.

The designs were completed within the MAGIC CAD Tools Environment and can be ported to multiple CAD systems and CMOS technologies.

All libraries are a single entry (metal1 to metal2 via) standard cell library for use in a full double level metal technology. Only metal1 is allowed within the cell boundary, with the exception of the I/O terminals (this does not hold true for the MSI cells and certain cells in dlmV2.0 where the reduced cell height has required the use of metal2 for nets). All unused channels are available for metal2 feedthru over the cell. All cells in dlmV2.0 are 66-lambda high.

The following pages describe the library members by cell name and description (function), and gives each cell's old name. In dlmV1.0, the IO cells were included in the SCMOS library. The IO cells are no longer provided as apart of dlmV1.1 or dlmV2.0, but are now provided as a separate library with separate documentation.

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Introduction

Version 2.0 of the Scalable CMOS (SCMOS) Standard Cell Library (dlmV2.0) is schematically equivalent to the original SCMOS library (dlmV1.0) released in December 1986 and version 1.1 (dlmV1.1) released in October 1988. The original version of the library was the result of a contract with USC-ISI to redesign the MOSIS CMOS3 (3 micron single metal) Standard Cell Library under MOSIS Scalable Design Rules. The development of dlmV1.1 and dlmV2.0 was performed under contract to UC, Berkeley as library support for their Lager IV Silicon Assembly System.

This updated version of the library features a reduced cell height from 100-lambda, in dlmV1.1, to 66-lambda. Also, dlmV2.0 exhibits “cornerless” transistors for increased manufacturability, as technologies are scaled down, and increased simulation accuracy. The additional area obtained from straightening the transistors was used for well plugs and guard rings to reduce susceptibility to latch-up. The new cell naming convention initiated with dlmV1.1 is used with dlmV2.0, as well. This document contains an explanation of the new naming convention and a cross reference of new names to old names.

Version 2.0 of the library can be obtained from the Advanced Microelectronics Division of the Institute for Technology Development (ITD/AμE) in MAGIC format under MOSIS Rev6 design rules and installed in the OCT database.

The functionality and performance of dlmV2.0 has been verified using SPICE-based tools developed at ITD/AμE. However, the contract did not provide for any silicon verification of the library.

ITD is a state and federally funded not-for-profit corporation. ITD/AμE cannot provide free consulting services. If you have a technical question, you may submit it in writing via mail or FAX, but there is no promise of any response.

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