Cell Name	Old Name	Cell Description
norf401	1140	4 Input NOR
oaif2201	1860	2, 2 OR/NAND Mux
orf401	1740	4 Input OR
pudf000	1440	Pull-Down
puuf000	1430	Pull-Up
swcf020	1370	Transmission Gate
via	8680	Wiring Via
xnof201	2350	Exclusive NOR
†xnsf201		Static Exclusive NOR
xorf201	2310	Exclusive OR
†xosf201		Static Exclusive NOR

† This cell uses a static CMOS implementation that can be simulated by IRSIM.

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Library Description

Cell Name	Old Name	Cell Description
aof2201	1970	2, 2 AND/OR Mux
aof2301	1930	2, 3 AND/OR Mux
aof3201	1810	3, 2 AND/OR Mux
aof4201	1910	4, 2 AND/OR Mux
aoif2201	1870	2, 2 AND/NOR Mux
blf00001	1880	2, 1 AND/NOR Mux
blf00101	1890	2, 1 OR/NAND Mux
buff100	1550	High Impedance Buffer
buff101	1320	Non-Inverting Buffer
buff121	1340	Tri-State Buffer
delf011	1560	Delay Cell
dfbf311	1480	D-Flip Flop with S, R, Q & QB
dfnf311	1830	D-Flip Flop with Q & QB
dfrf301	1570	D-Flip Flop with Asynchronous R & Q
dfrf311	1580	D-Flip Flop with Asynchronous R, Q & QB
faf001	1850	Full Adder
feed	8630	Buss Crosser
invf100	1540	High Impedance Inverter
invf101	1310	Inverter
invf103	1330	3X Inverting Buffer
invf104	1520	4X Inverting Buffer
invf201	1100	Dual Inverter
labf111	1410	NAND Latch
labf211	1420	NOR Latch
larf310	1530	Clocked Latch
ldf001	8660	RC Load Cell
muxf201	1350	Data Select
nanf201	1220	2 Input NAND
nanf211	1660	2 Input NAND/AND
nanf251	1620	A OR B-not Decoder
nanf301	1230	3 Input NAND
nanf311	1670	3 Input NAND/AND
nanf401	1240	4 Input NAND
nanf411	1680	4 Input NAND/AND
norf201	1120	2 Input NOR
norf211	1760	2 Input OR/NOR
norf251	1610	A-not AND B Decoder
norf301	1130	3 Input NOR
norf311	1770	3 Input OR/NOR

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