********** SPICE DECK **********

*** Generated from aof2201.mag by magic's spice generator
*** technology: scmos
*** timestamp: 598556309
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x36 120 A1 54 vdd PMOS W=31.0U L=2.0U
M16x36 54 51 120 vdd PMOS W=31.0U L=2.0U
M24x36 120 52 vdd vdd PMOS W=31.0U L=2.0U
M32x36 vdd 53 120 vdd PMOS W=31.0U L=2.0U
M48x36 vdd 54 O vdd PMOS W=31.0U L=2.0U
M8x10 gnd A1 150 gnd NMOS W=11.0U L=2.0U
M12x10 150 51 54 gnd NMOS W=11.0U L=2.0U
M20x10 54 52 151 gnd NMOS W=11.0U L=2.0U
M28x10 151 53 gnd gnd NMOS W=11.0U L=2.0U
M48x1 gnd 54 O gnd NMOS W=25.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.82	3.56	4.00	7.83
	Pd 1--0	2.71	4.08	5.96	8.98
	Tr 0--1	1.78	4.37	3.92	9.61
	Tf 1--0	0.95	2.60	2.09	5.72
C2,D2---O	Pd 0--1	1.82	3.56	4.00	7.83
	Pd 1--0	2.71	4.08	5.96	8.98
	Tr 0--1	1.78	4.37	3.92	9.61
	Tf 1--0	0.95	2.60	2.09	5.72

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	5.21	7.27	10.10	13.31
	Pd 1--0	6.65	8.25	12.51	15.57
	Tr 0--1	3.37	6.96	5.96	10.08
	Tf 1--0	2.86	4.28	3.61	7.18
C2,D2---O	Pd 0--1	5.21	7.27	10.10	13.31
	Pd 1--0	6.65	8.25	12.51	15.57
	Tr 0--1	3.37	6.96	5.96	10.08
	Tf 1--0	2.86	4.28	3.61	7.18

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	11	2
51	11	2
52	11	2
53	11	2
54	25	2
24	31	2
20	31	2
21	31	2
22	31	2
23	31	2

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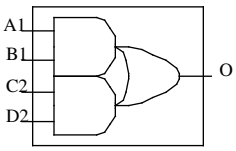
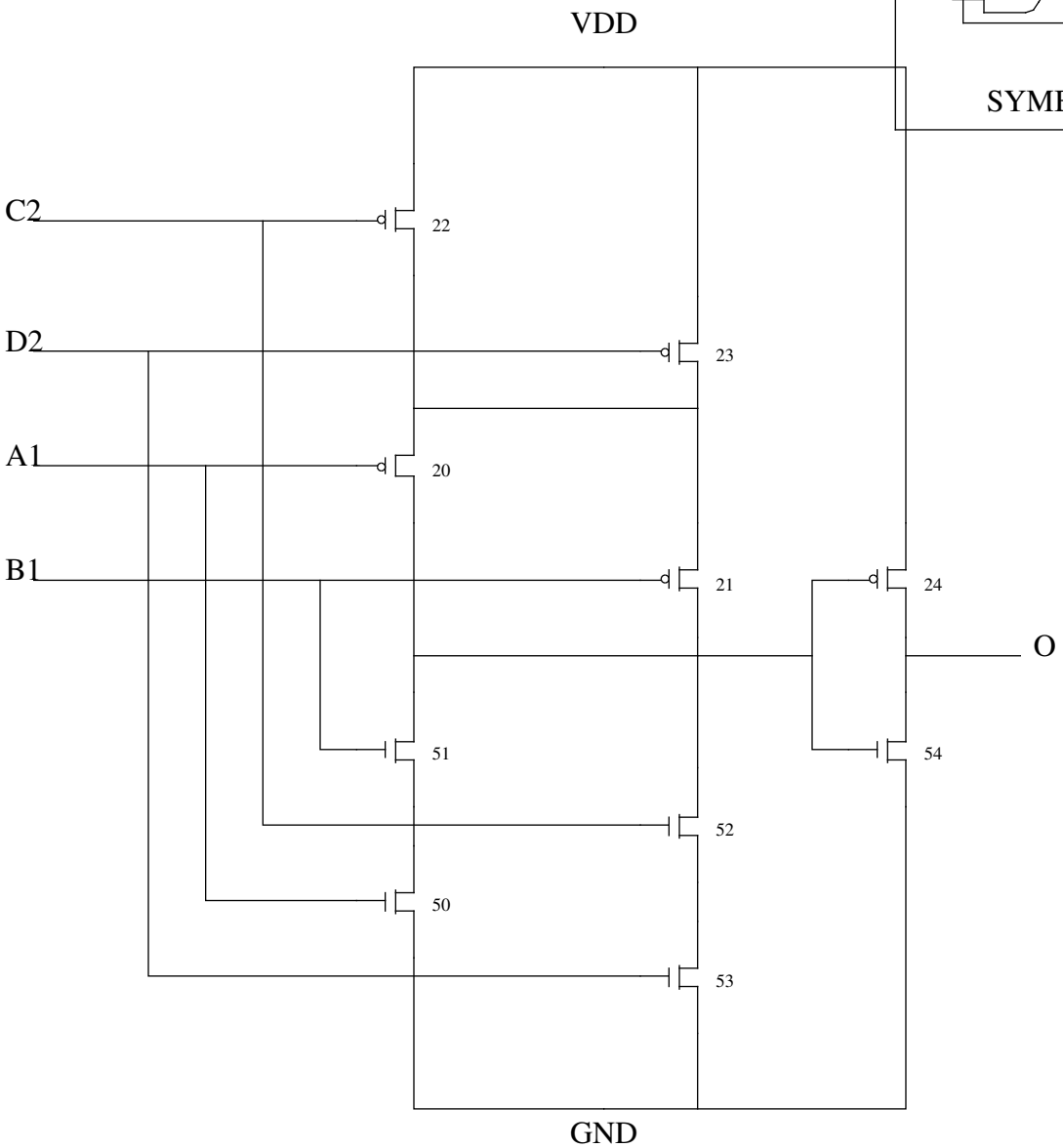
ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**aof2201** 2/2_AND/OR_MUX	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	30	1
2	B1	32	1
3	FeedThru	----	----
4	C2	32	2
5	D2	32	2
6	FeedThru	----	----
7	O	30	0

LOGIC EQUATIONS: O = AB + CD

Truth Table

AB	CD	O
-	1	1
1	-	1