********** SPICE DECK **********

*** Generated from aof3201.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x47 120 50 26 vdd PMOS W=23.0U L=2.0U
M16x47 26 51 120 vdd PMOS W=23.0U L=2.0U
M24x46 120 C2 121 vdd PMOS W=24.0U L=2.0U
M32x47 121 D2 120 vdd PMOS W=23.0U L=2.0U
M52x47 vdd E3 121 vdd PMOS W=23.0U L=2.0U
M60x47 121 F3 vdd vdd PMOS W=23.0U L=2.0U
M72x47 vdd 26 O vdd PMOS W=23.0U L=2.0U
M12x4 26 50 150 gnd NMOS W=22.0U L=2.0U
M16x4 150 51 gnd gnd NMOS W=22.0U L=2.0U
M32x4 gnd C2 151 gnd NMOS W=23.0U L=2.0U
M36x4 151 D2 26 gnd NMOS W=23.0U L=2.0U
M44x4 26 E3 152 gnd NMOS W=24.0U L=2.0U
M50x4 152 F3 gnd gnd NMOS W=22.0U L=2.0U
M69x4 gnd 26 O gnd NMOS W=22.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.80	4.03	3.96	8.87
	Pd 1--0	3.01	4.46	6.62	9.81
	Tr 0--1	1.50	5.33	3.30	11.73
	Tf 1--0	0.95	3.27	2.09	7.19
C2,D2---O	Pd 0--1	2.22	4.51	4.88	9.92
	Pd 1--0	2.99	4.67	6.58	10.27
	Tr 0--1	1.17	5.33	2.57	11.73
	Tf 1--0	1.06	3.38	2.33	7.44
E3,F3---O	Pd 0--1	2.68	4.78	5.90	10.52
	Pd 1--0	3.17	4.77	6.97	10.49
	Tr 0--1	2.03	5.35	4.47	11.77
	Tf 1--0	1.11	3.25	2.44	7.15

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	5.57	8.24	10.92	14.87
	Pd 1--0	7.51	9.63	13.91	17.72
	Tr 0--1	3.38	8.85	6.29	12.23
	Tf 1--0	2.98	5.43	5.33	7.58
C2,D2---O	Pd 0--1	6.61	9.31	12.42	17.20
	Pd 1--0	8.35	10.95	14.84	18.90
	Tr 0--1	3.69	8.98	6.36	13.37
	Tf 1--0	3.46	5.43	4.62	8.36
E3,F3---O	Pd 0--1	6.97	9.86	13.99	18.37
	Pd 1--0	9.61	12.44	16.28	20.23
	Tr 0--1	4.35	9.31	6.91	13.40
	Tf 1--0	3.27	5.23	4.22	8.47

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
56	22	2
52	23	2
53	23	2
54	24	2
55	22	2
50	22	2
51	22	2
20	23	2
21	23	2
22	24	2
23	23	2
26	23	2
25	23	2
24	23	2

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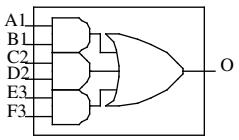
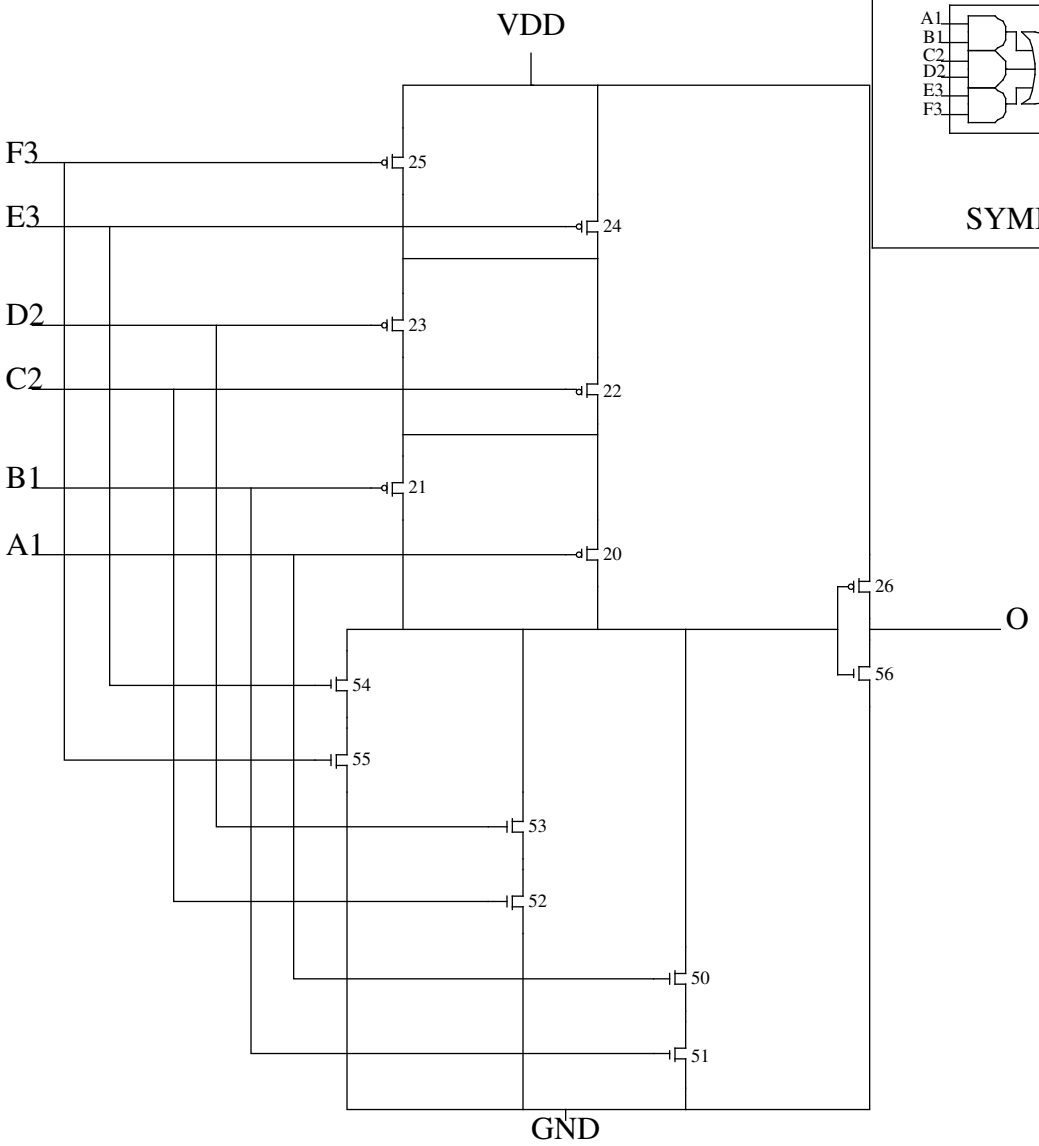
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**aof3201** 3/2_AND/OR	DATE: Mar 11,1989 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	36	1
2	FeedThru	----	----
3	B1	41	1
4	C2	38	2
5	D2	35	2
6	FeedThru	----	----
7	E3	38	3
8	F3	33	3
9	FeedThru	----	----
10	O	35	0

LOGIC EQUATIONS: O = AB + CD + EF

Truth Table

AB	CD	EF	O
-	-	1	1
-	1	-	1
1	-	-	1