********** SPICE DECK **********

*** Generated from aoif2201.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598548256
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x39 120 D2 O vdd PMOS W=28.0U L=2.0U
M16x39 O 52 120 vdd PMOS W=28.0U L=2.0U
M24x39 120 B1 vdd vdd PMOS W=28.0U L=2.0U
M32x39 vdd A1 120 vdd PMOS W=28.0U L=2.0U
M12x4 gnd D2 151 gnd NMOS W=12.0U L=2.0U
M16x4 151 52 O gnd NMOS W=12.0U L=2.0U
M24x4 O B1 150 gnd NMOS W=12.0U L=2.0U
M28x4 150 A1 gnd gnd NMOS W=12.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.91	5.20	4.20	11.44
	Pd 1--0	2.36	5.04	5.19	11.09
	Tr 0--1	3.47	8.67	7.63	19.07
	Tf 1--0	2.92	7.51	6.42	16.52
C2,D2---O	Pd 0--1	1.91	5.20	4.20	11.44
	Pd 1--0	1.46	4.62	3.21	10.16
	Tr 0--1	2.99	8.67	6.58	19.07
	Tf 1--0	1.89	6.68	4.16	14.70

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	5.14	9.24	9.90	16.83
	Pd 1--0	5.75	9.33	13.30	19.12
	Tr 0--1	7.55	16.12	13.73	23.94
	Tf 1--0	8.00	14.33	14.33	22.86
C2,D2---O	Pd 0--1	5.14	9.24	9.90	16.83
	Pd 1--0	4.01	7.82	9.62	16.41
	Tr 0--1	7.55	16.12	13.29	23.94
	Tf 1--0	4.65	10.63	9.84	18.02

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
52	12	2
51	12	2
50	12	2
53	12	2
23	28	2
22	28	2
21	28	2
20	28	2

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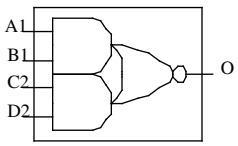
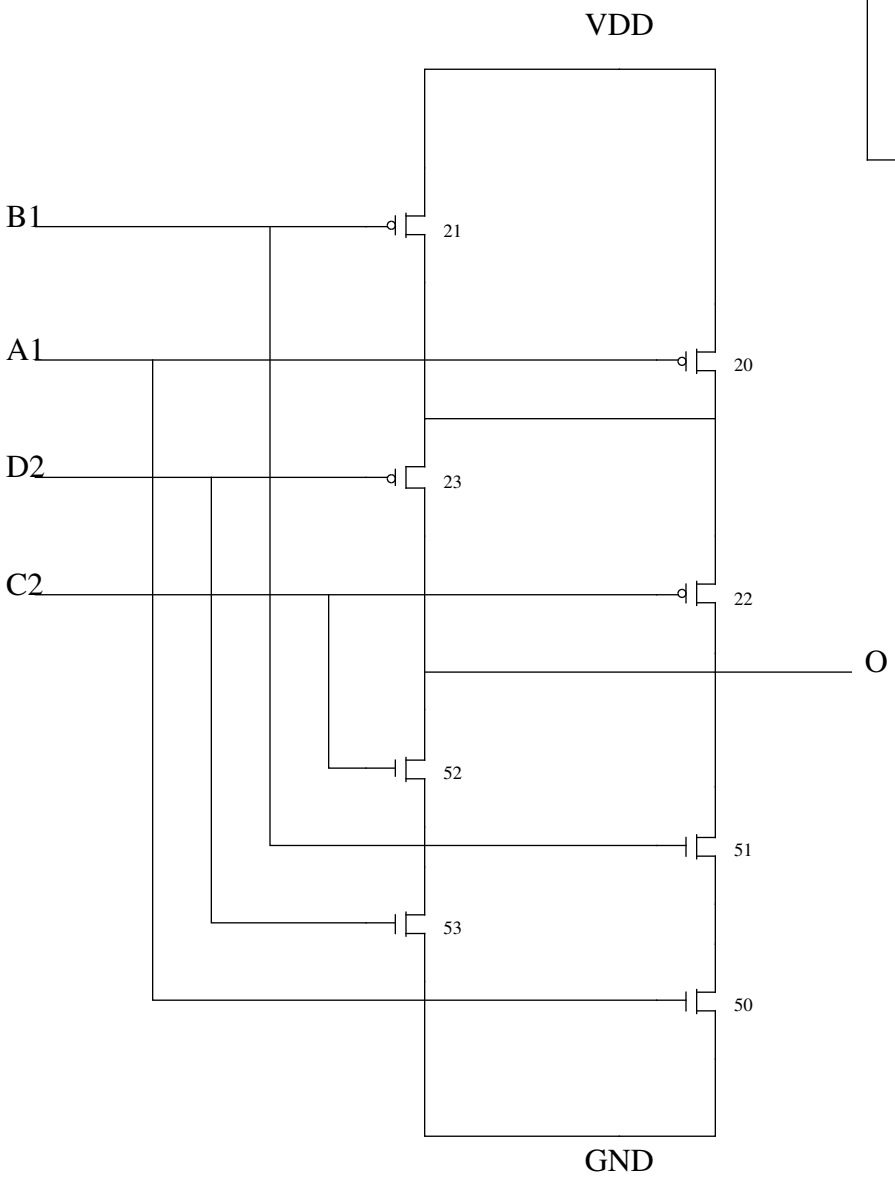
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**aoif2201** 2/2_AND/NOR_MUX	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	D2	34	2
2	O	35	0
3	C2	33	2
4	B1	23	1
5	A1	29	1

LOGIC EQUATIONS: O = (AB + CD)'

Truth Table

AB	CD	O
0	0	1