********** SPICE DECK **********

*** Generated from blf00001.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598548348
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x40 O 50 120 vdd PMOS W=27.0U L=2.0U
M16x40 120 51 vdd vdd PMOS W=27.0U L=2.0U
M24x40 vdd 52 120 vdd PMOS W=27.0U L=2.0U
M8x10 gnd 50 O gnd NMOS W=6.0U L=2.0U
M16x5 O 51 150 gnd NMOS W=11.0U L=2.0U
M20x5 150 52 gnd gnd NMOS W=11.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.51	5.15	3.32	11.33
	Pd 1--0	1.15	4.96	2.53	10.91
	Tr 0--1	3.11	8.97	6.84	19.73
	Tf 1--0	2.39	7.52	5.26	16.54
B2,C2---O	Pd 0--1	1.51	5.15	3.32	11.33
	Pd 1--0	1.96	5.05	4.31	11.11
	Tr 0--1	3.11	8.97	6.84	19.73
	Tf 1--0	2.50	7.45	5.50	16.39

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	4.02	8.81	7.54	16.05
	Pd 1--0	2.83	7.15	6.88	15.00
	Tr 0--1	7.03	16.20	12.92	25.25
	Tf 1--0	4.55	10.50	10.21	18.84
B2,C2---O	Pd 0--1	4.02	8.81	7.54	16.05
	Pd 1--0	4.76	8.74	11.53	18.54
	Tr 0--1	7.03	16.20	12.92	25.25
	Tf 1--0	5.05	10.84	10.52	19.00

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	11	2
52	11	2
50	6	2
21	27	2
20	27	2
22	27	2

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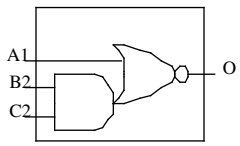
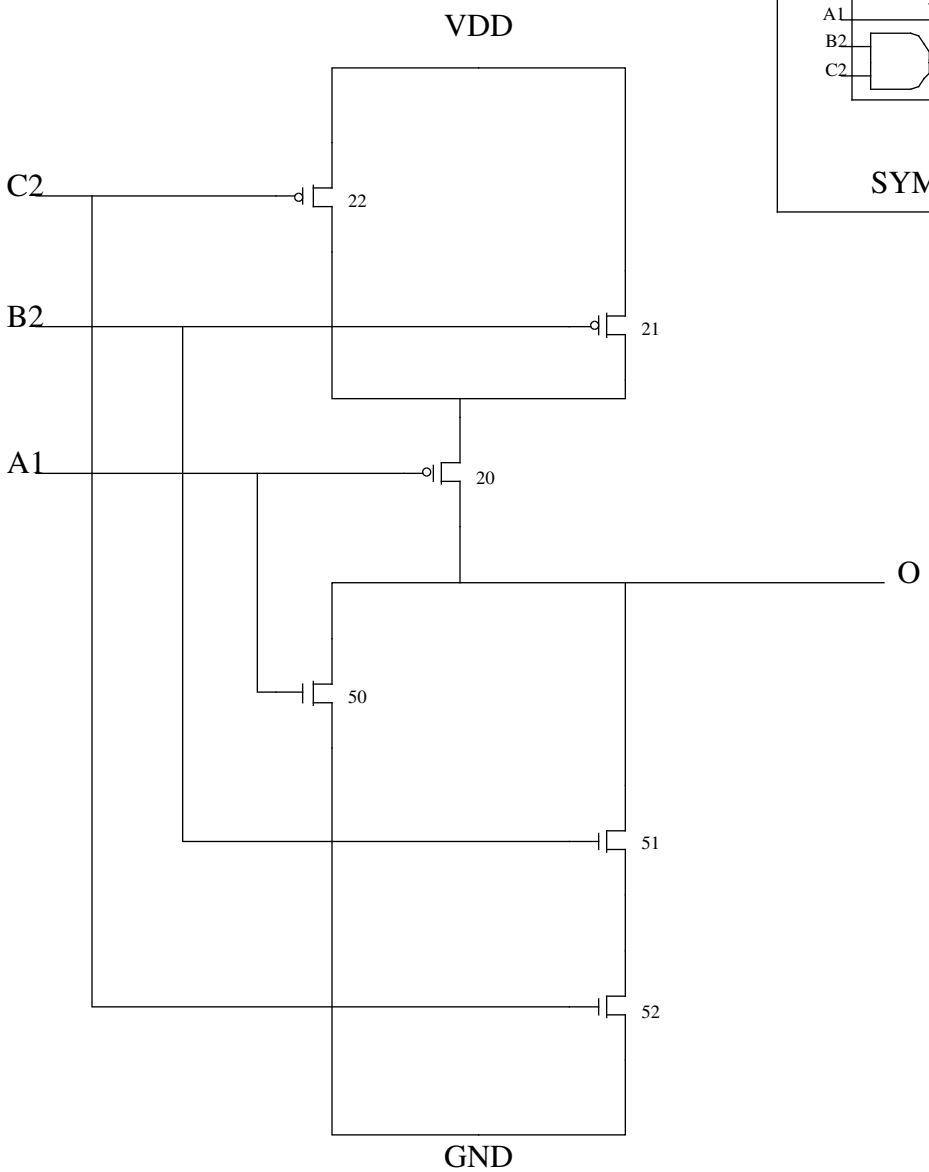
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**blf00001** 2/1_AND/NOR_MUX	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	31	1
2	O	36	0
3	B2	22	2
4	C2	29	2

LOGIC EQUATIONS: O = (A + BC)'

Truth Table

A	BC	O
0	0	1