********** SPICE DECK **********

*** Generated from blf00101.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598548551
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x42 vdd A1 O vdd PMOS W=25.0U L=2.0U
M16x36 O 51 120 vdd PMOS W=31.0U L=2.0U
M20x36 120 52 vdd vdd PMOS W=31.0U L=2.0U
M8x1 gnd A1 150 gnd NMOS W=20.0U L=2.0U
M16x10 150 51 O gnd NMOS W=11.0U L=2.0U
M24x10 O 52 150 gnd NMOS W=11.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.39	3.59	3.06	7.90
	Pd 1--0	1.59	4.33	3.50	9.53
	Tr 0--1	3.09	6.69	6.80	14.72
	Tf 1--0	2.05	5.97	4.51	13.13
B2,C2---O	Pd 0--1	1.54	4.71	3.39	10.36
	Pd 1--0	1.59	4.33	3.50	9.53
	Tr 0--1	3.01	7.64	6.62	16.81
	Tf 1--0	2.05	5.97	4.51	13.13

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	3.72	6.26	7.19	12.09
	Pd 1--0	4.11	7.21	10.02	15.78
	Tr 0--1	7.32	11.49	12.99	20.36
	Tf 1--0	4.54	9.45	9.54	17.29
B2,C2---O	Pd 0--1	4.27	8.26	8.04	15.07
	Pd 1--0	4.11	7.21	10.02	15.78
	Tr 0--1	7.32	13.07	12.44	23.14
	Tf 1--0	4.54	9.45	9.54	17.29

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	20	2
52	11	2
51	11	2
22	31	2
21	31	2
20	25	2

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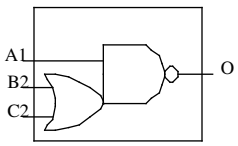
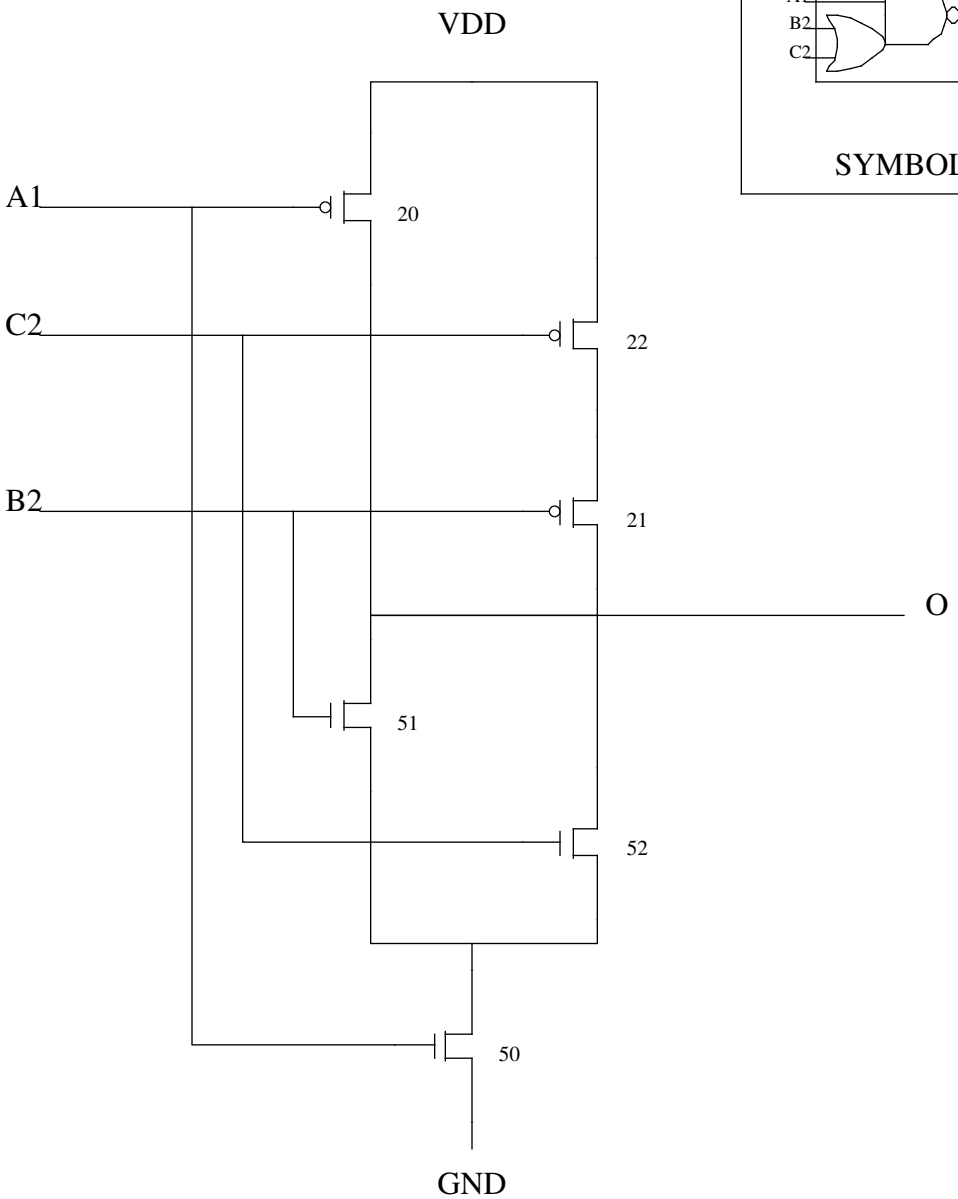
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**blf00101** 2/1_OR/NAND_MUX	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	32	1
2	B2	27	2
3	O	25	0
4	C2	31	2

LOGIC EQUATIONS: O = (A * (B+C))'

Truth Table

A	B	C	O
0	-	-	1
-	0	0	1