Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**buff100** HI_Z_BUFFER	DATE: Mar 11,1989 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from buff100.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x43 O 52 vdd vdd PMOS W=18.0U L=2.0U
M27x48 120 50 52 vdd PMOS W=14.0U L=7.0U
M8x11 O 52 gnd gnd NMOS W=14.0U L=2.0U
M24x11 gnd vdd 150 gnd NMOS W=8.0U L=2.0U
M28x11 150 50 52 gnd NMOS W=8.0U L=6.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	3.57	6.43	7.85	14.15
	Pd 1--0	4.28	6.83	9.42	15.03
	Tr 0--1	1.56	6.50	3.43	14.30
	Tf 1--0	1.79	4.64	3.94	10.21

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	9.31	13.37	17.54	23.62
	Pd 1--0	11.58	15.40	21.85	28.10
	Tr 0--1	4.01	11.14	6.45	14.82
	Tf 1--0	5.59	9.17	7.53	12.61

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
52	14	2
50	8	6
20	14	7
22	18	2

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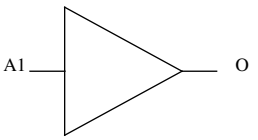
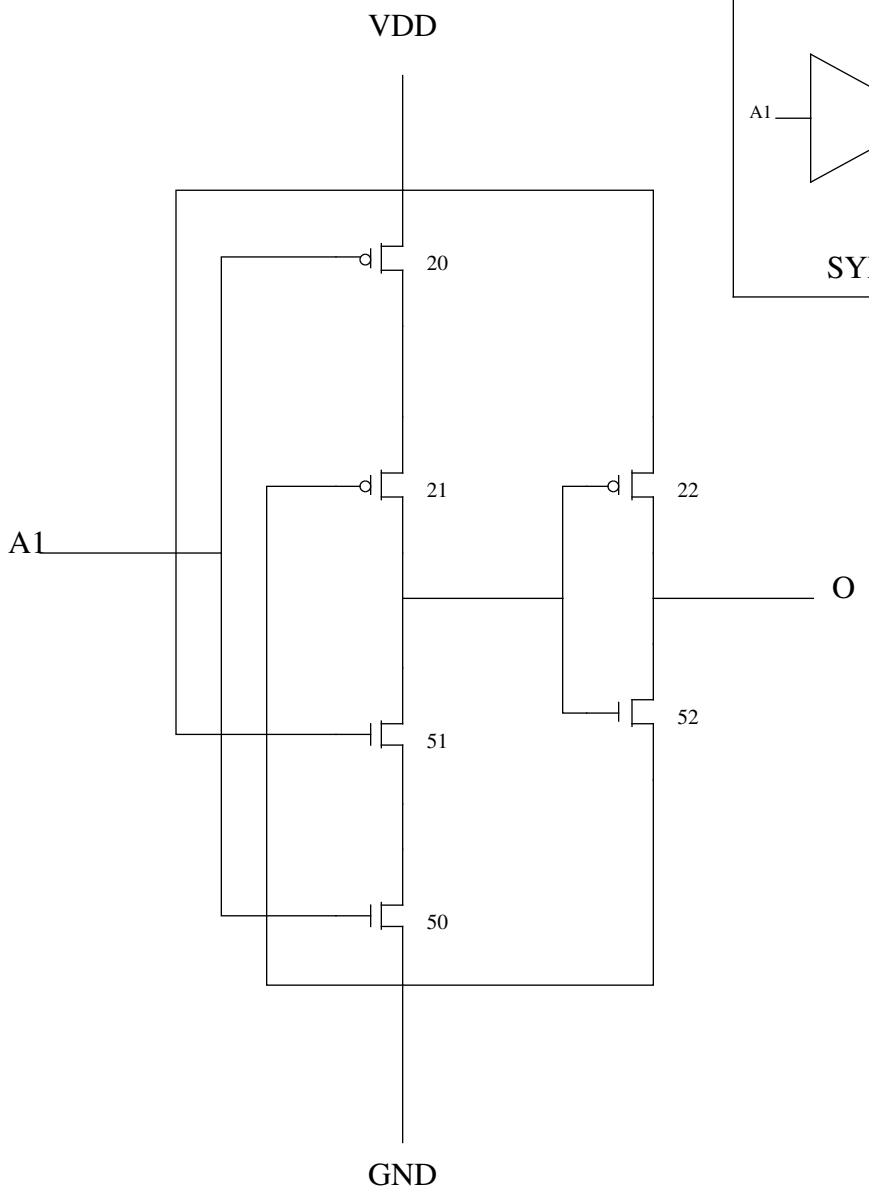


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	O	39	0
2	FeedThru	----	----
3	FeedThru	----	----
4	A1	42	1
5	FeedThru	----	----

LOGIC EQUATIONS: O = A

Truth Table

A	O
1	1