Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**buff101** NON_INVERTING_BUFFER	DATE: Dec 21,1988 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from buff101.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598317886
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x36 51 50 vdd vdd PMOS W=22.0U L=2.0U
M16x36 vdd 51 O vdd PMOS W=31.0U L=2.0U
M8x11 51 50 gnd gnd NMOS W=9.0U L=2.0U
M16x7 gnd 51 O gnd NMOS W=13.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.22	2.82	2.68	6.20
	Pd 1--0	1.26	2.85	2.77	6.27
	Tr 0--1	1.36	4.22	2.99	9.28
	Tf 1--0	1.17	3.69	2.57	8.12

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	3.41	5.46	6.79	10.41
	Pd 1--0	3.50	5.81	6.03	9.76
	Tr 0--1	2.64	6.53	3.44	9.28
	Tf 1--0	2.30	5.47	3.70	8.60

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	9	2
51	13	2
21	31	2
20	22	2

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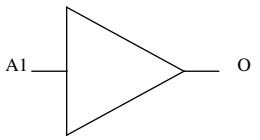
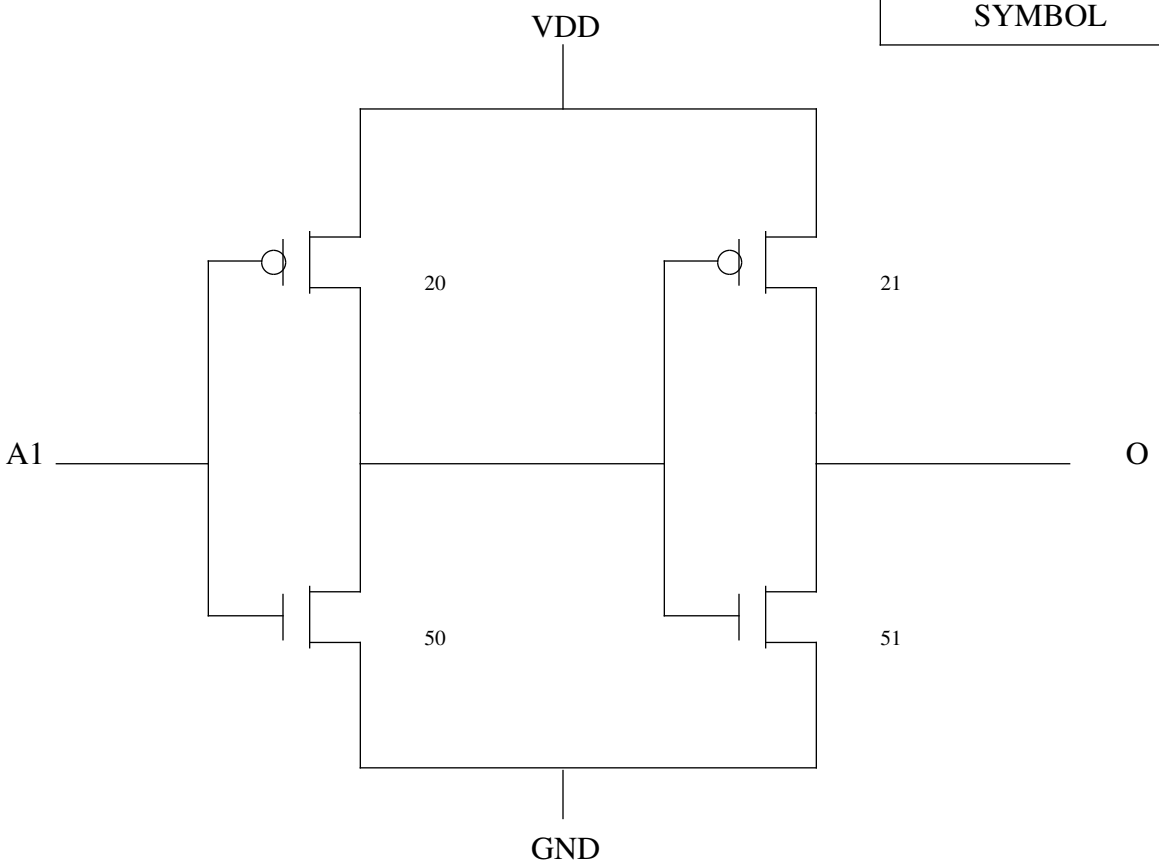


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	A1	38	1
3	O	32	0

LOGIC EQUATIONS: O = A

Truth Table

A	O
1	1