********** SPICE DECK **********

*** Generated from buff121.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598318072
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x41 50 52 vdd vdd PMOS W=26.0U L=2.0U
M16x41 vdd 52 24 vdd PMOS W=26.0U L=2.0U
M25x36 24 50 54 vdd PMOS W=23.0U L=2.0U
M47x39 24 51 vdd vdd PMOS W=28.0U L=2.0U
M56x39 vdd 24 O vdd PMOS W=28.0U L=2.0U
M8x1 50 52 gnd gnd NMOS W=24.0U L=2.0U
M16x1 gnd 50 54 gnd NMOS W=16.0U L=2.0U
M24x1 54 52 24 gnd NMOS W=24.0U L=2.0U
M48x1 54 51 gnd gnd NMOS W=24.0U L=2.0U
M56x1 gnd 54 O gnd NMOS W=24.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
DATA1---O	Pd 0--1	1.00	2.87	2.20	6.31
	Pd 1--0	2.04	3.57	4.49	7.85
	Tr 0--1	0.88	4.58	1.94	10.08
	Tf 1--0	0.99	2.67	2.18	5.87
EN2---O	Pd 0--1	0.37	2.42	0.81	5.32
	Pd 1--0	0.52	1.48	1.14	3.26
	Tr 0--1	1.03	4.43	2.27	9.75
	Tf 1--0	0.61	2.09	1.34	4.60

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
DATA1---O	Pd 0--1	3.84	6.24	7.14	10.81
	Pd 1--0	5.54	7.79	11.51	14.98
	Tr 0--1	2.82	7.31	4.99	10.33
	Tf 1--0	2.53	4.85	5.35	7.33
EN2---O	Pd 0--1	2.29	4.97	4.09	8.33
	Pd 1--0	2.77	4.85	5.56	8.28
	Tr 0--1	3.30	7.25	4.97	10.08
	Tf 1--0	2.49	4.39	3.40	5.89

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
53	24	2
54	24	2
51	24	2
50	16	2
52	24	2
20	26	2
22	26	2
24	28	2
21	28	2
23	23	2

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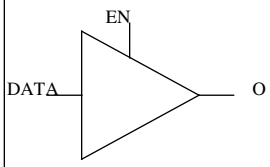
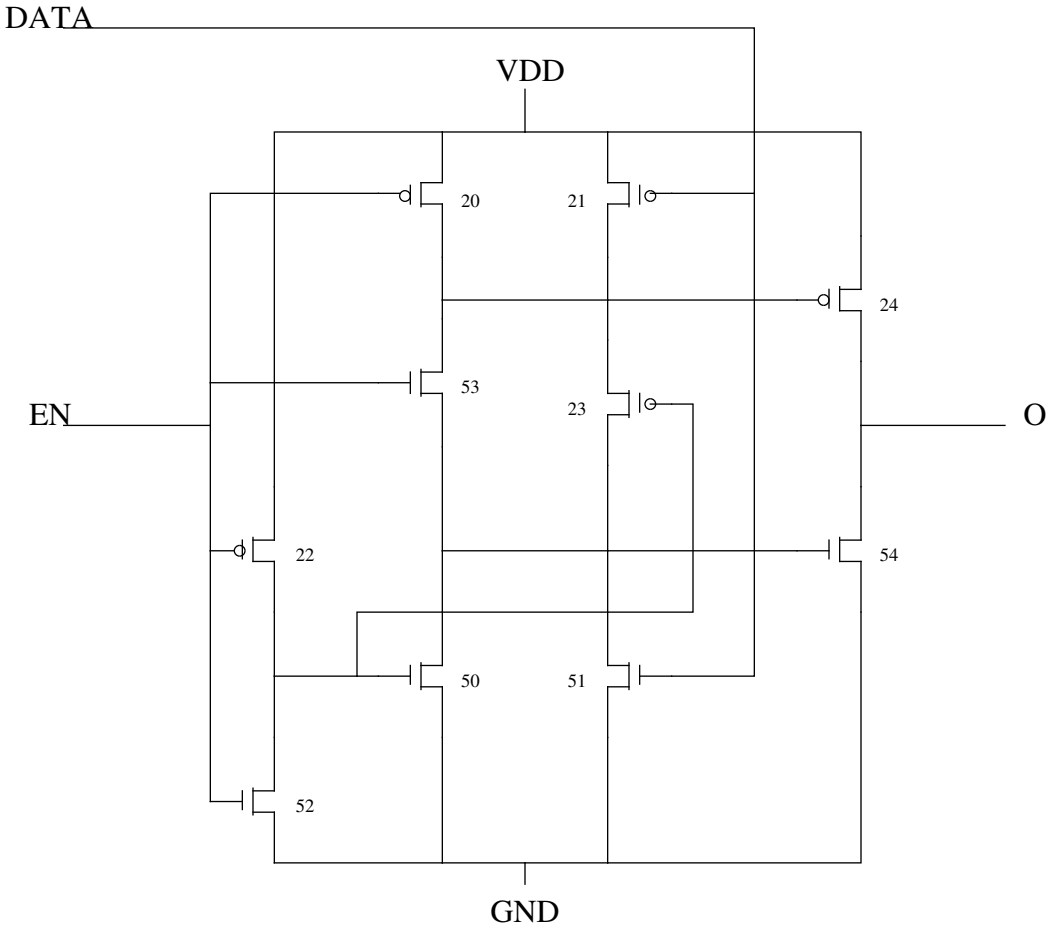
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**buff121** TRI_STATE_BUFFER	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	EN2	31	2
2	FeedThru	----	----
3	FeedThru	----	----
4	FeedThru	----	----
5	DATA1	36	1
6	FeedThru	----	----
7	FeedThru	----	----
8	O	35	0

LOGIC EQUATIONS: See Truth Table

Truth Table

EN	D	O
0	-	Z
1	0	0
1	1	1