Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**delf011** DELAY_CELL	DATE: Dec 21,1988 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from delf011.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598319207
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M21x47 vdd 51 120 vdd PMOS W=10.0U L=5.0U
M30x47 120 gnd 23 vdd PMOS W=20.0U L=2.0U
M6x41 vdd 50 51 vdd PMOS W=11.0U L=5.0U
M45x41 vdd 23 54 vdd PMOS W=7.0U L=5.0U
M60x44 vdd 54 O vdd PMOS W=23.0U L=2.0U
M9x16 51 50 gnd gnd NMOS W=4.0U L=5.0U
M38x20 54 23 gnd gnd NMOS W=4.0U L=8.0U
M18x9 gnd 51 150 gnd NMOS W=6.0U L=8.0U
M28x9 150 vdd 23 gnd NMOS W=6.0U L=2.0U
M52x12 gnd 54 O gnd NMOS W=12.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	13.82	16.61	30.40	36.54
	Pd 1--0	13.44	16.12	29.57	35.46
	Tr 0--1	2.10	6.18	4.62	13.60
	Tf 1--0	2.15	5.31	4.73	11.68

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	37.39	41.40	59.83	65.54
	Pd 1--0	36.26	40.01	59.23	65.23
	Tr 0--1	7.00	12.54	8.95	16.13
	Tf 1--0	6.29	10.35	8.04	14.63

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	4	5
51	6	8
54	12	2
53	4	8
52	6	2
20	11	5
21	10	5
22	20	2
24	23	2
23	7	5

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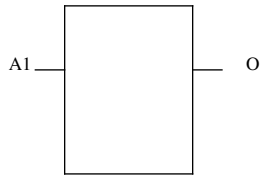
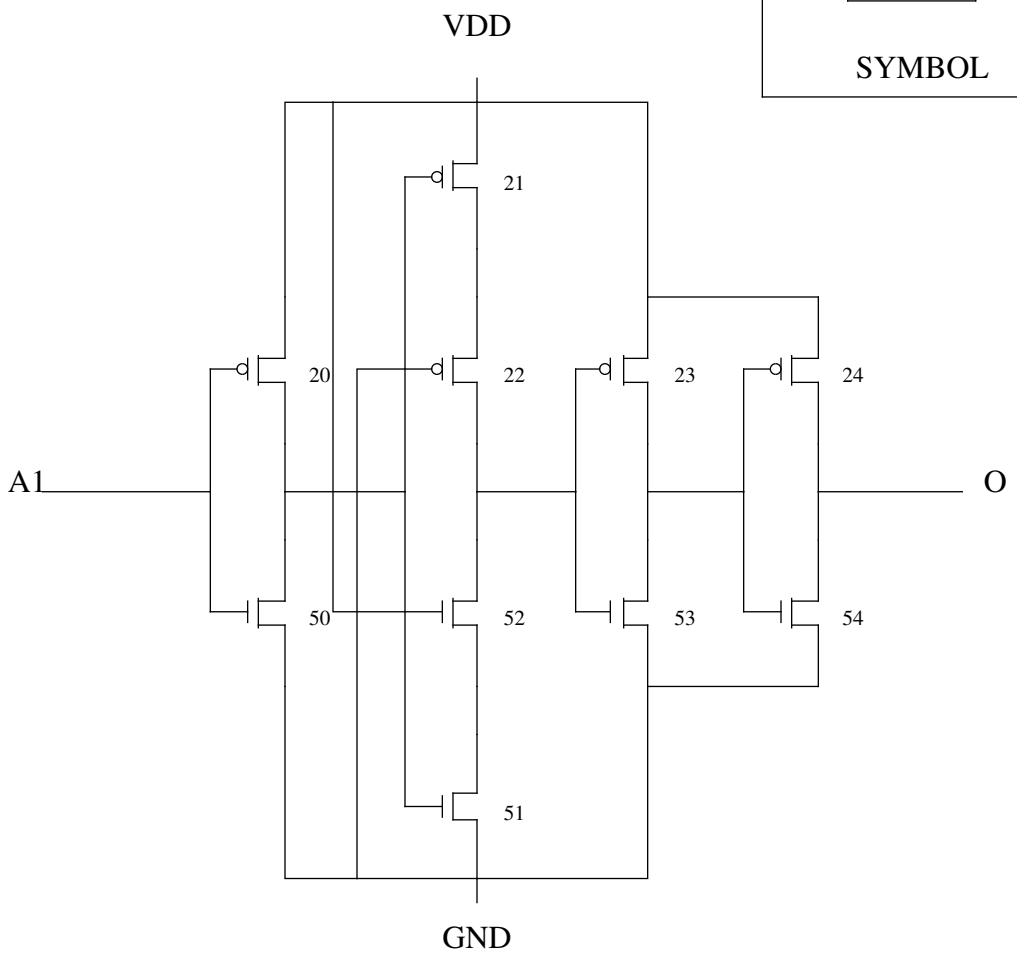


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	25	1
2	FeedThru	----	----
3	FeedThru	----	----
4	FeedThru	----	----
5	FeedThru	----	----
6	FeedThru	----	----
7	FeedThru	----	----
8	O	27	0

LOGIC EQUATIONS: O = A

Truth Table

A	O
1	1